

Selecting Decoupling Capacitors for Flat Impedance

Heidi Barnes

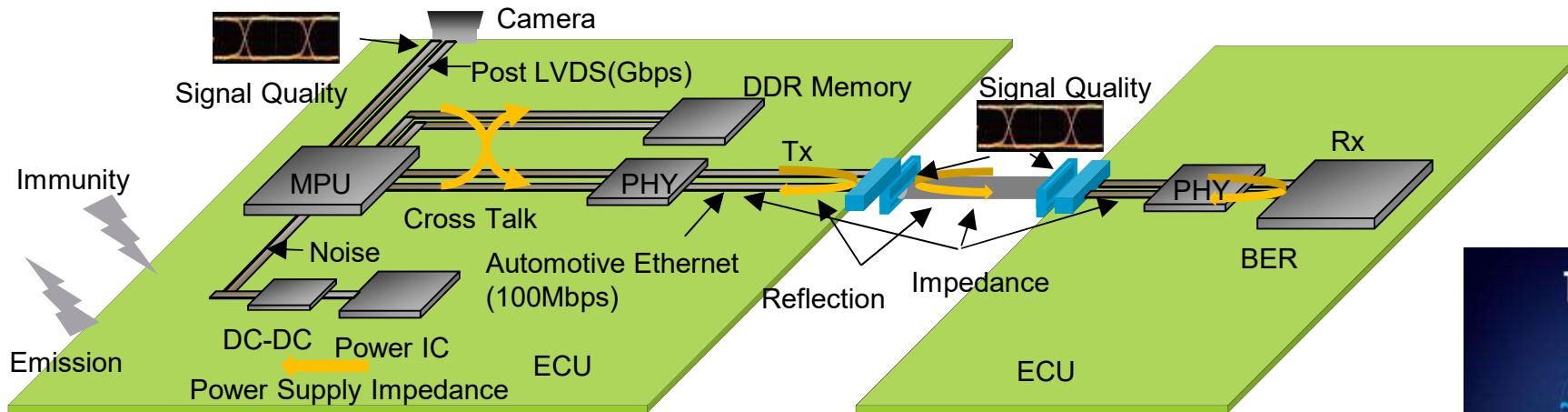
2020.3.12

Keysight Power Integrity Applications Expert



SI is the Goal, PI is the Foundation

PI is not DC - Fast delivery of power at microwave frequencies

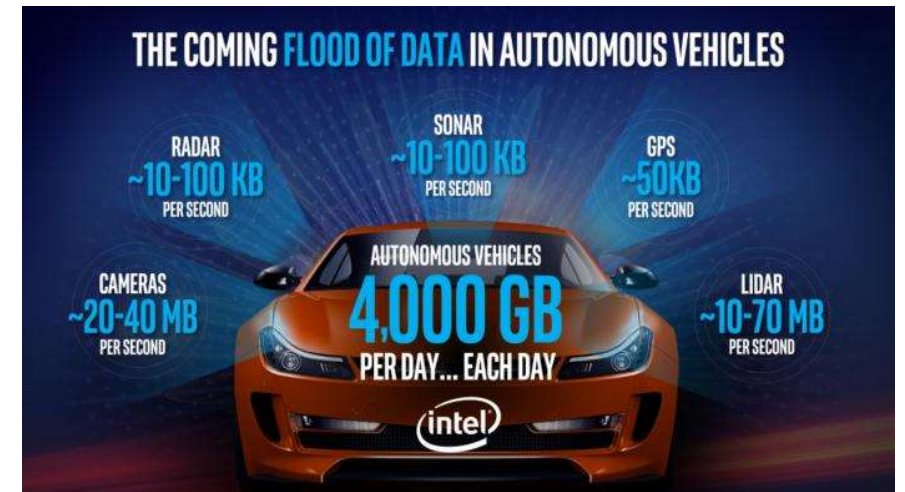


Key Take Away:

Power Integrity Engineers need RF/uW design and measurement tools!

Power Delivery Eco-System

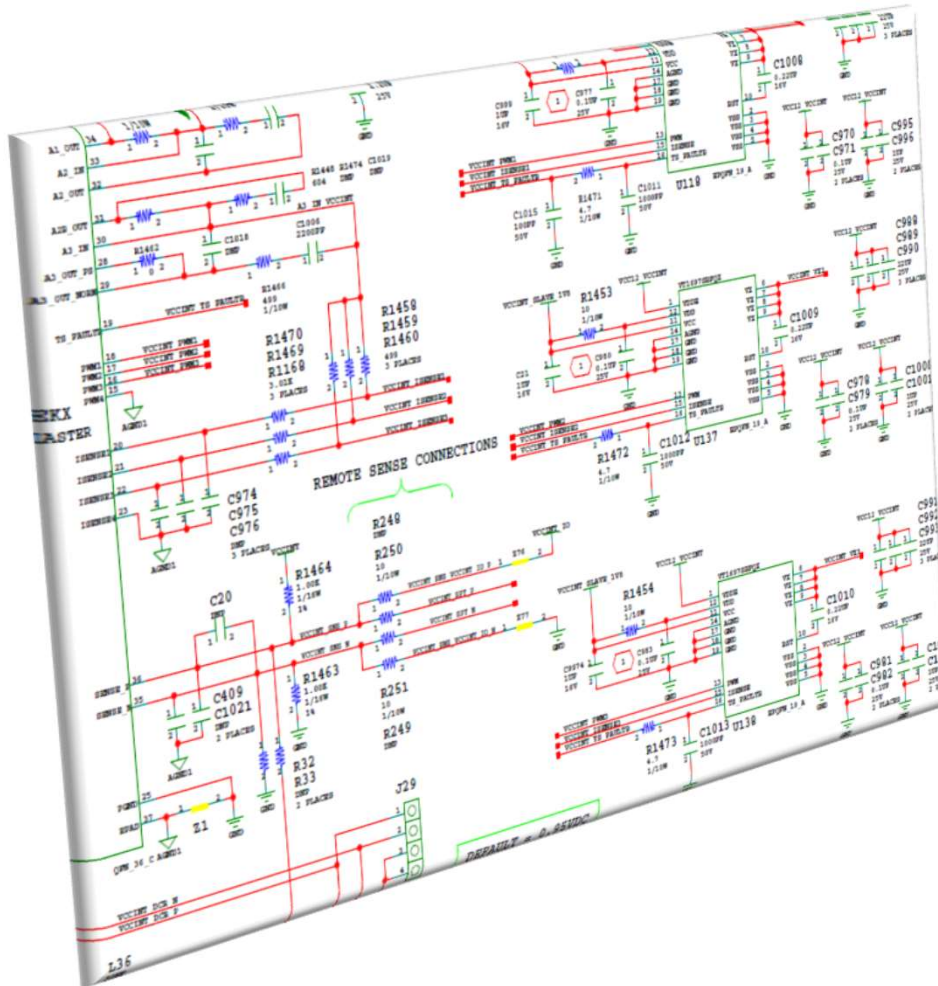
- Many Point-of-Load power supplies
- Low Voltage, High $\frac{dI}{dt}$ Switching Loads
- Target Z to reduce broadband $L \frac{dI}{dt}$ Voltage Noise
- Power Supply Rejection Ration (PSRR)
- DC-DC Converter Switching Noise and Stability



Note: A Point-of-Load (POL) Power Supply is typically a Switched Mode Power Supply (SMPS) with a Buck Regulator DC-DC Converter design that the Microprocessor PCB world often calls as a Voltage Regulator Module (VRM)

Electrical Schematics vs. Layout

Power is the foundation that connects to everything



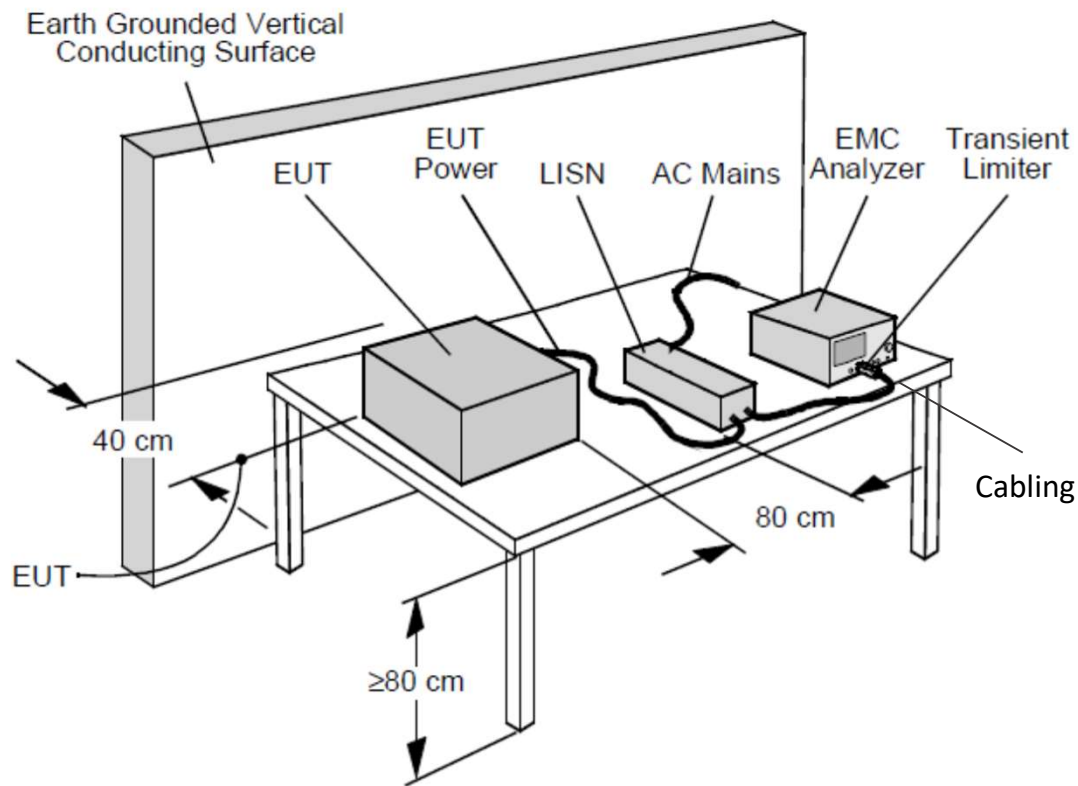
Modern High Density Electronics

- 1000s of nets
- A web of interconnected point of load power supplies
- 1 ground net
 - Barely noticeable on a schematic
 - Typically the largest copper net in layout
 - Noise path connected to everything

Failing EMI is Expensive

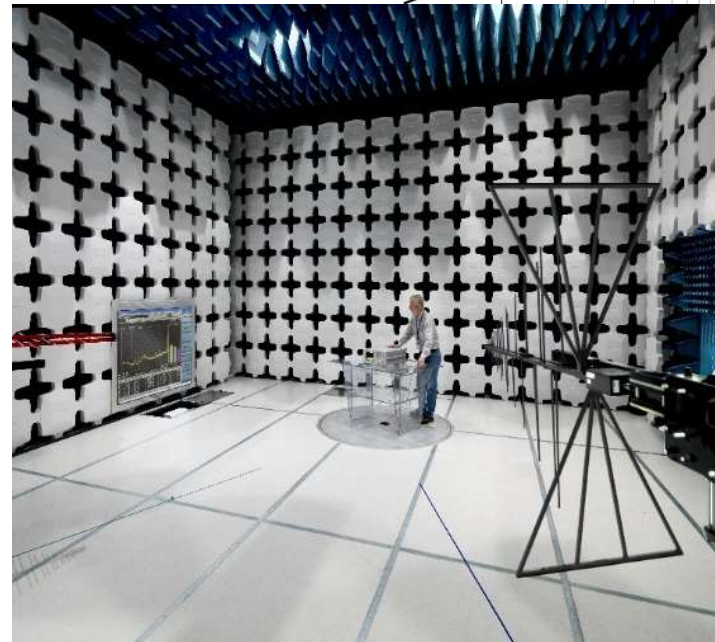
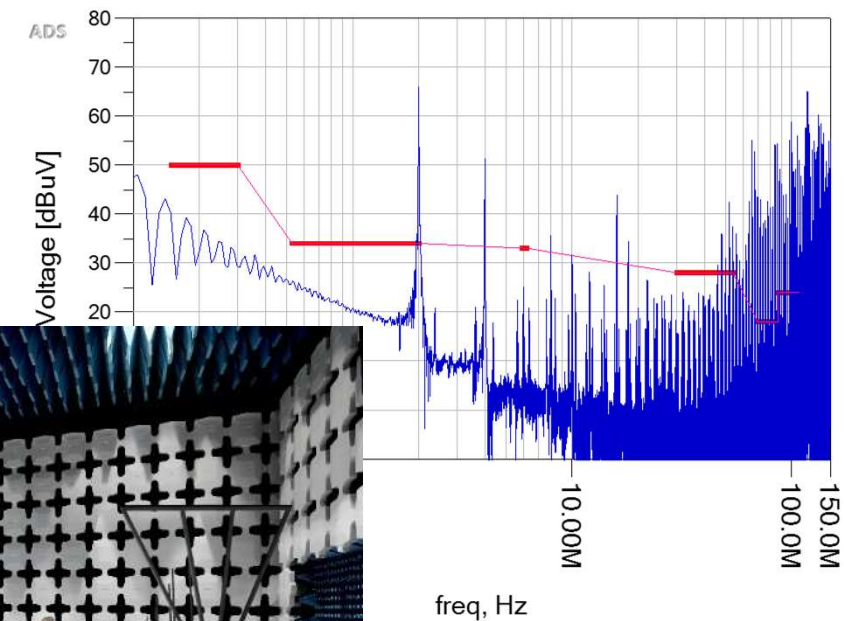
Final Product must pass EMI/EMC regulations

Conducted Emission Testing



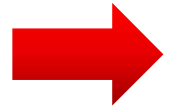
CISPR Compliance

CISPR 25, Class 5 Compliance: Differential Noise (peak)



3 Step Decoupling Capacitor Optimization

Design Methodology for DeCap Optimization

- 
1. Calculate 1st order approximations using simple resistor, inductor, capacitor **R-L-C** models
 2. Use **Target Z** to optimize the decoupling capacitor selection using high fidelity EM models (**ADS PIPro**)
 3. Validate with full **Power Integrity Eco-System** simulation in ADS

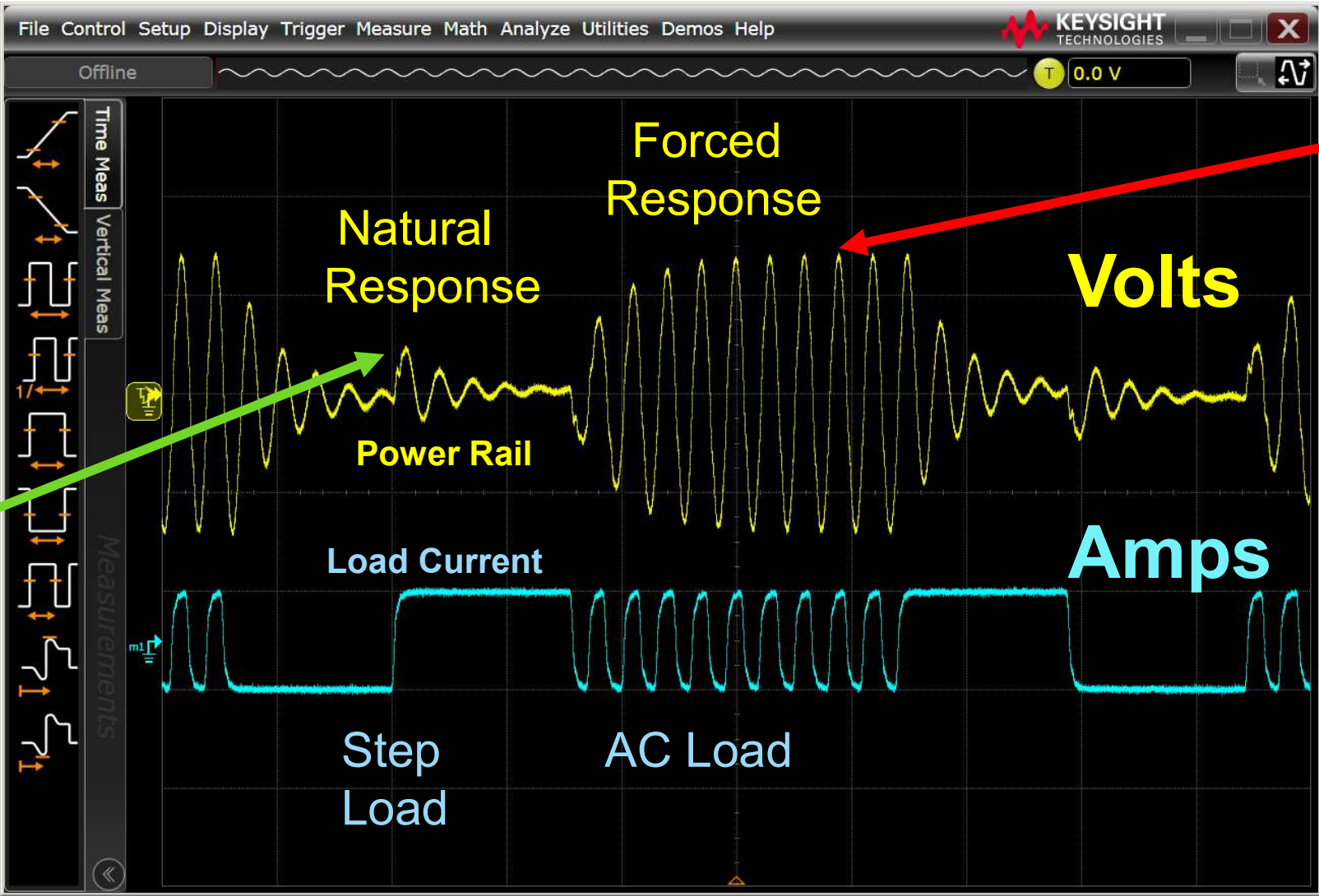
Old Methods Fail to Detect Worst Case Failures

Data Tx/Rx Failure, Over Voltage, EMI/EMC, Crosstalk

$$V = L \frac{dI}{dt}$$

Old Method:
Step Load
Transient Test
(False Positive)

PASS
Datasheet
Design

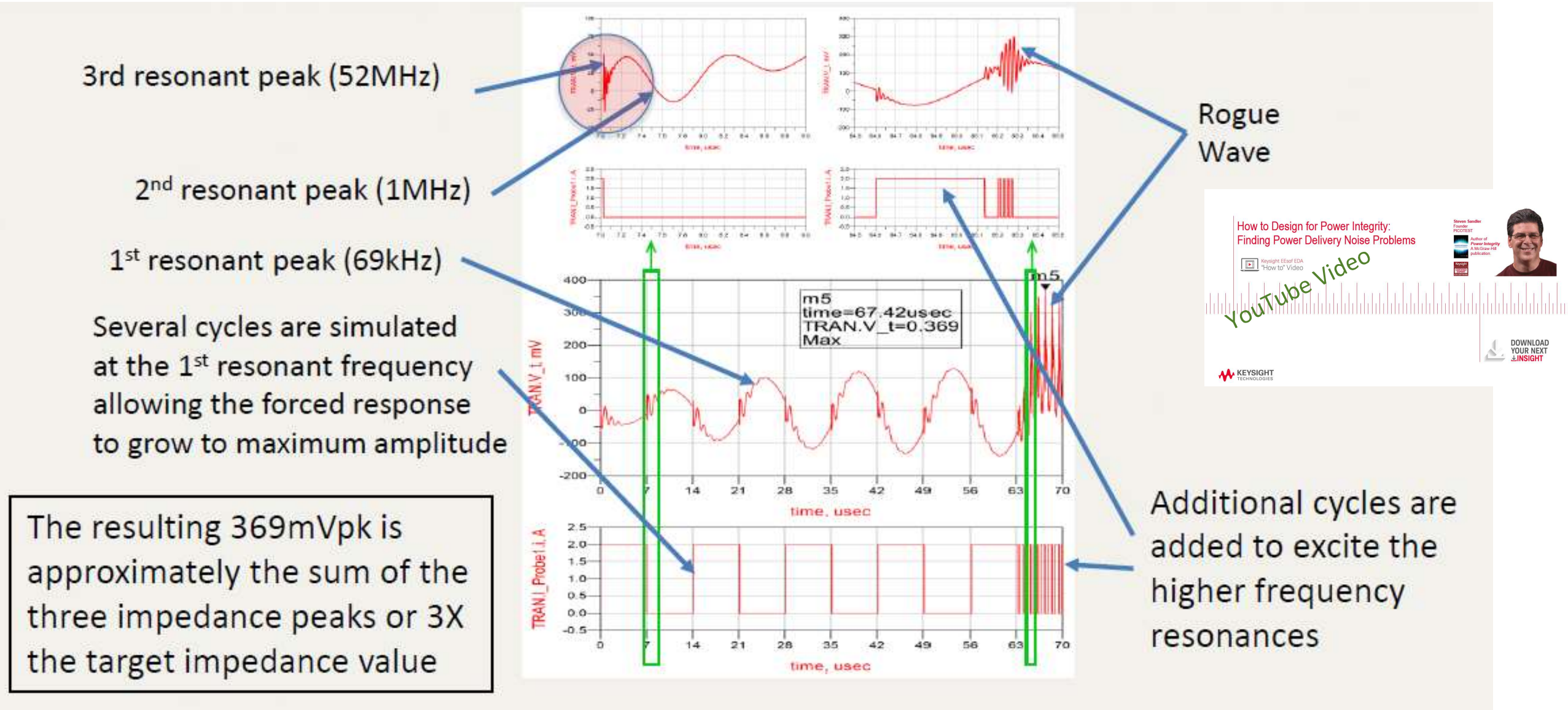


New Method:
Finding the
worst case Load

FAIL
Over Voltage
Tx/Rx Bit Error
EMI
Crosstalk

Key Take Away:
Forced response *is*
worst case, not the
data sheet step load.

Finding the Rogue Wave

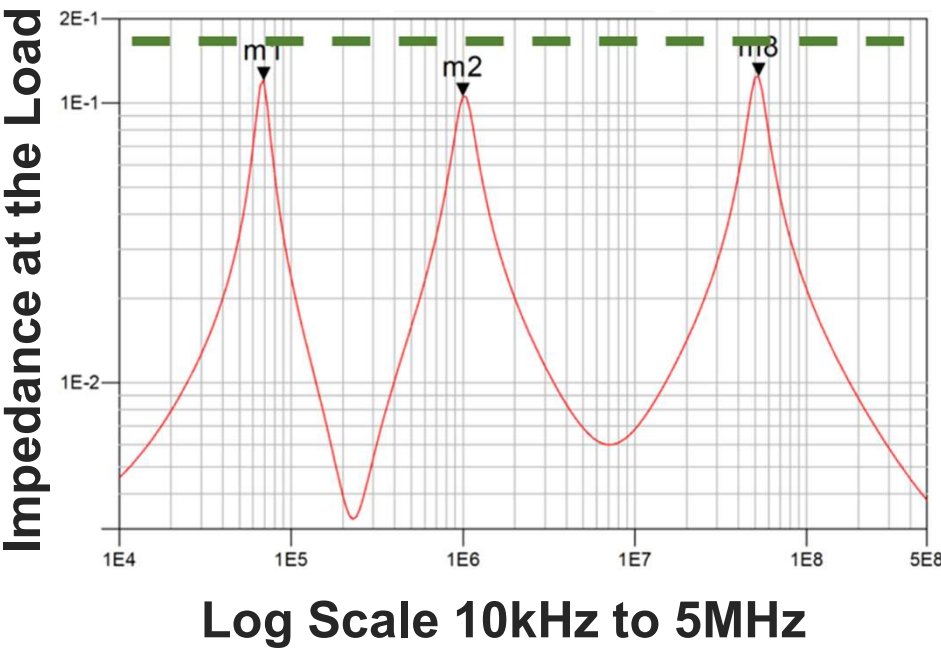


Power Rail Impedance is the New Way!

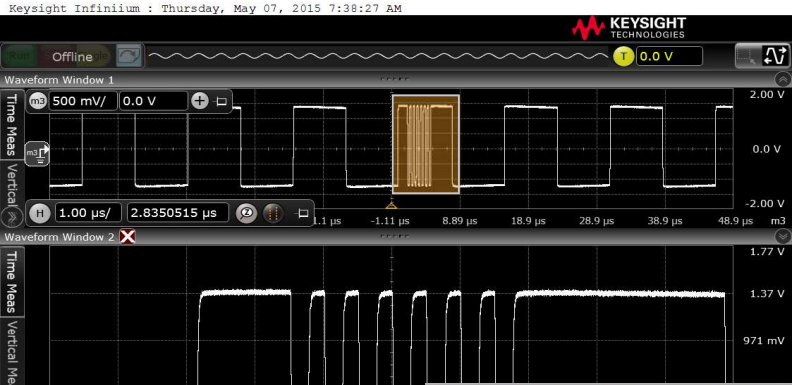
Impedance peaks in the frequency domain cause power rail ripple

$$V_{\text{ripple}} = I_{\text{transient}} * Z_{\text{pdn}}$$

Impedance Peaks Help Predict Worst Case Load Transients

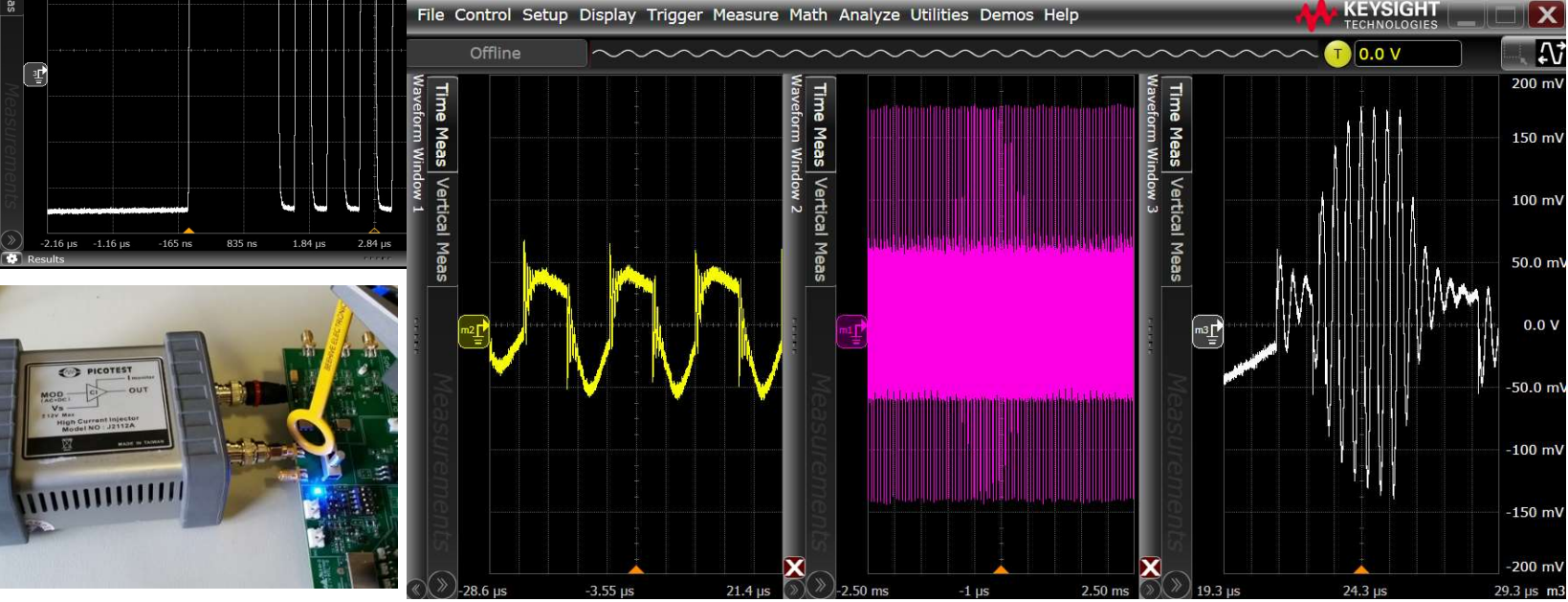


Forced Excitation at Peak Z Frequencies



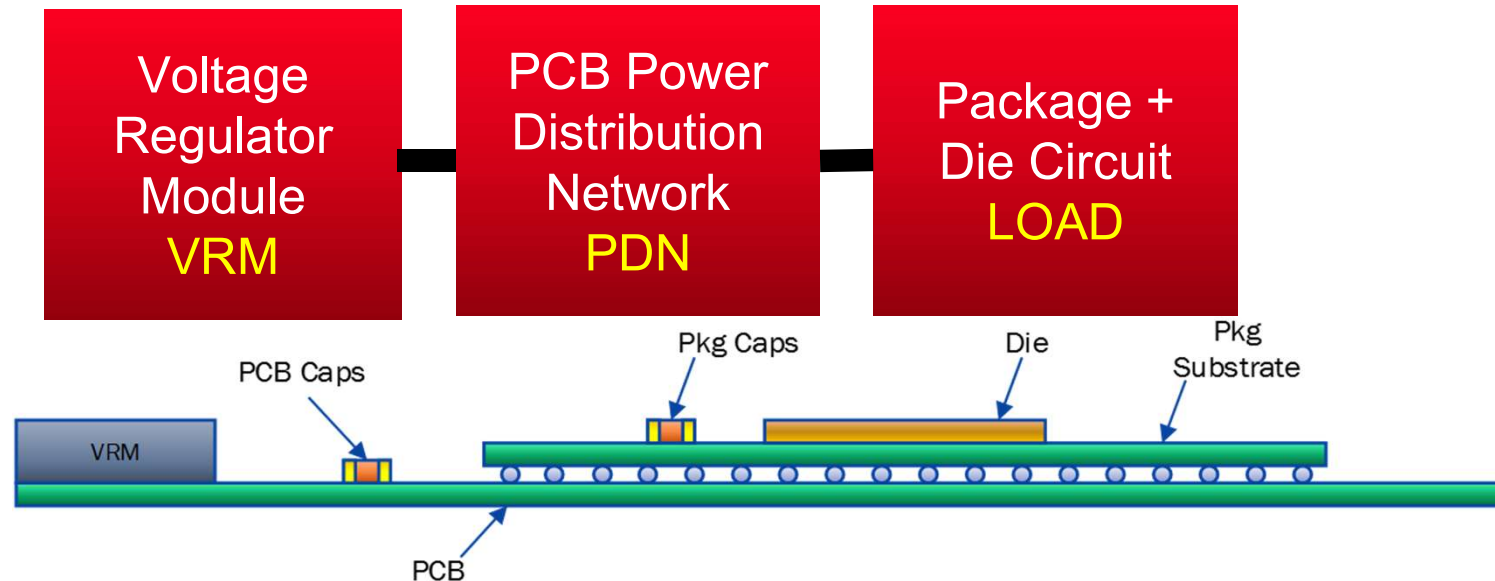
Key Take Away:
Voltage Rogue Waves are Real

Rogue Wave Captured



Power Integrity Target Impedance

Target Z times delta current transient is the max voltage ripple



Target Impedance Calculation

$$Z_{\text{Target}} = \frac{\Delta V_{\text{Max Ripple}}}{\Delta I_{\text{Max Transient Load}}}$$

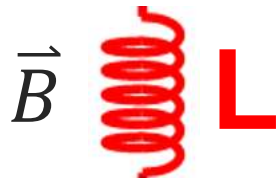
Where does the ringing come from?

Energy swings between the L and the C

*Energy stored in
the Magnetic Field*

$$V(t) = L \frac{di}{dt}$$

$$Z = j\omega L$$

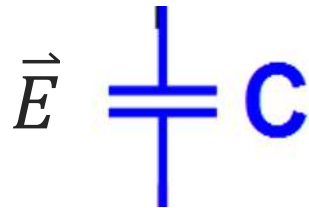


Phase V Leads I

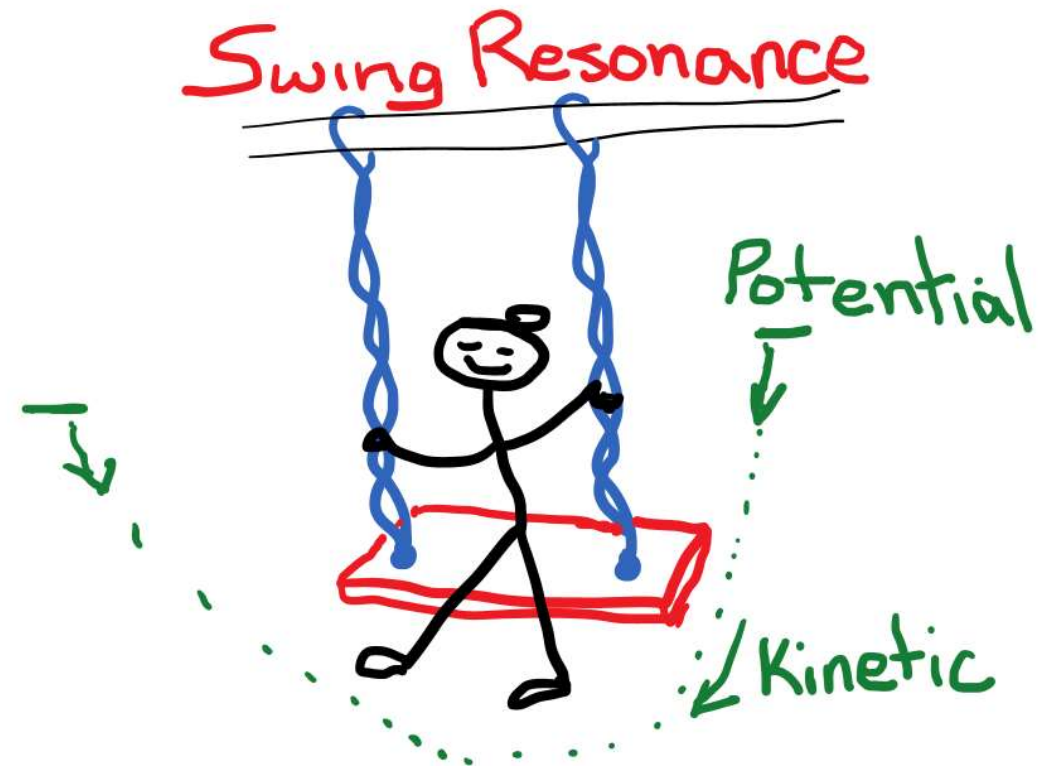
*Energy stored in
the Electric Field*

$$I = \int C \frac{dV}{dt}$$

$$Z = \frac{-1}{j\omega C}$$



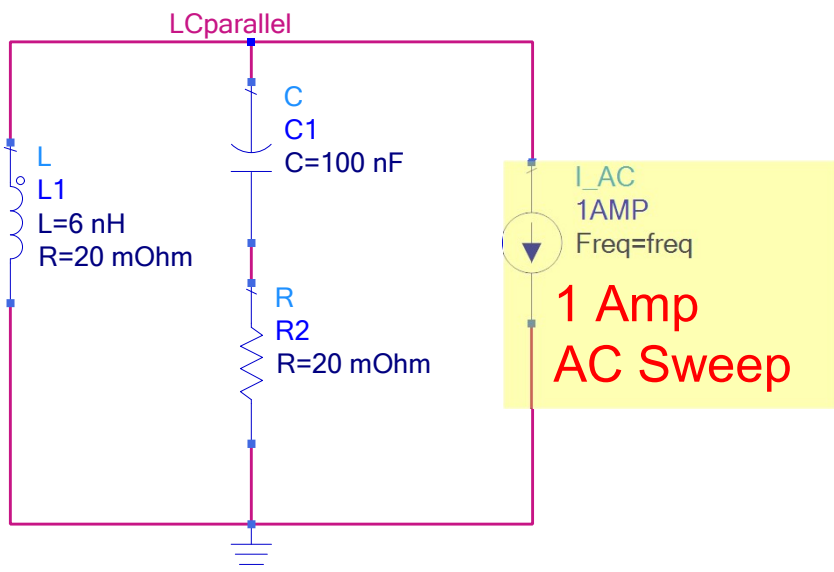
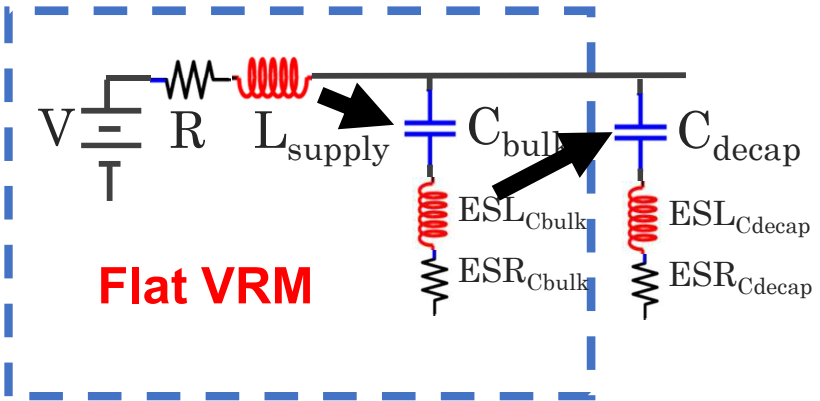
Phase V Lags I



Root Cause of Ringing on the Power Rail

Parallel inductance can resonate with the decoupling capacitance

Parallel L-C in the PDN



$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

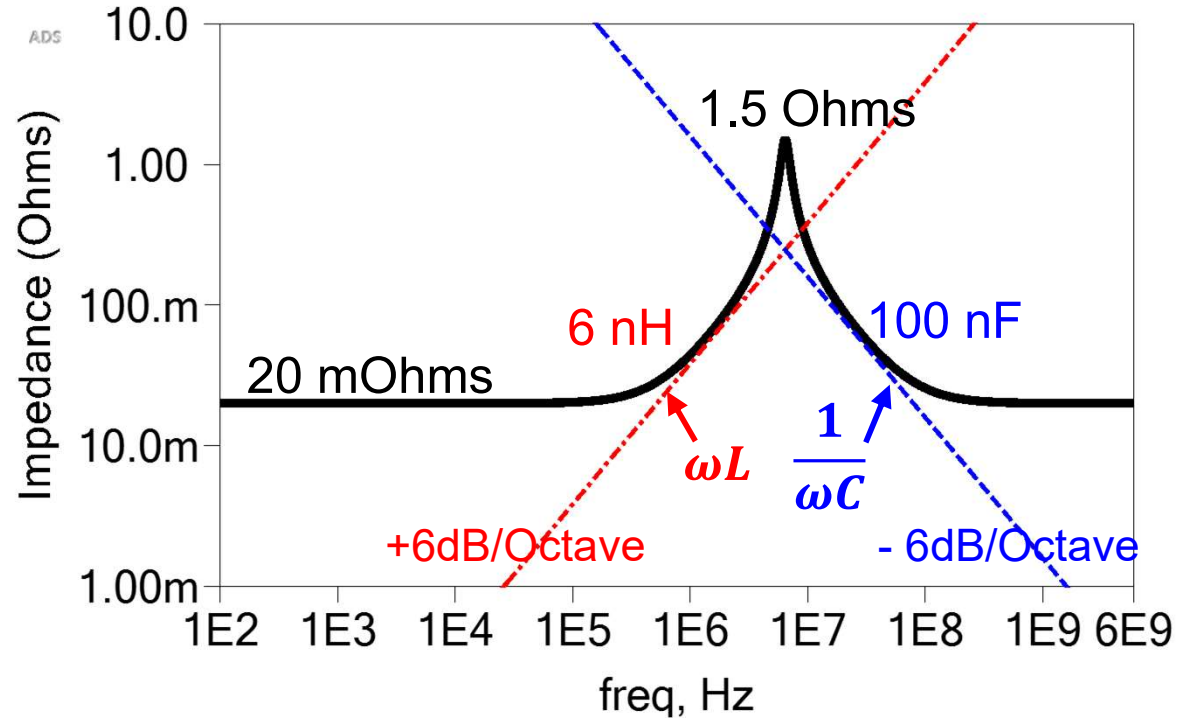
$$\Delta V = \Delta I \cdot Z_{peak}$$

$$Z_{peak} = Z_0 \cdot Q$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

$$Q = \frac{Z_0}{R_{total}}$$

Impedance vs. Frequency



$Z_{peak} = 1.5 \text{ Ohms}$

$Z_0 = 250 \text{ mOhms}$

Bandwidth of the Power Supply Control Loop f_{supply}

Decoupling is required to extend the Power supply bandwidth

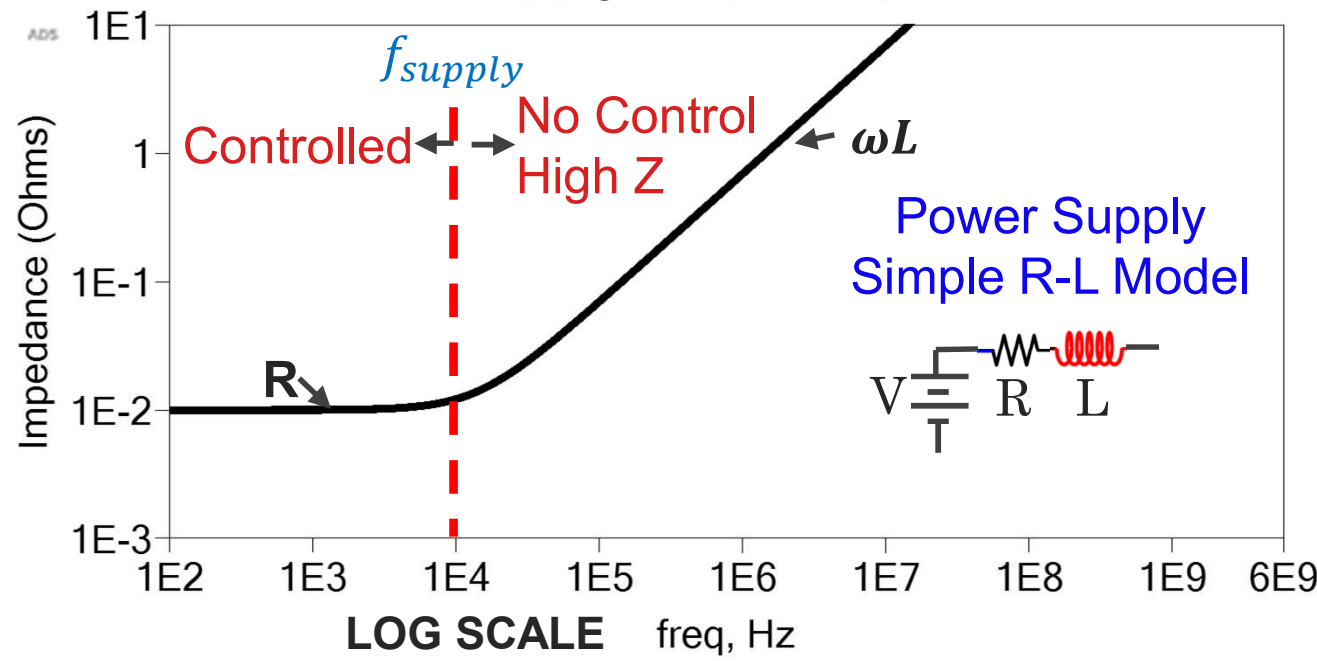
PROBLEM

The Load can make the Power Supply Control Loop go unstable

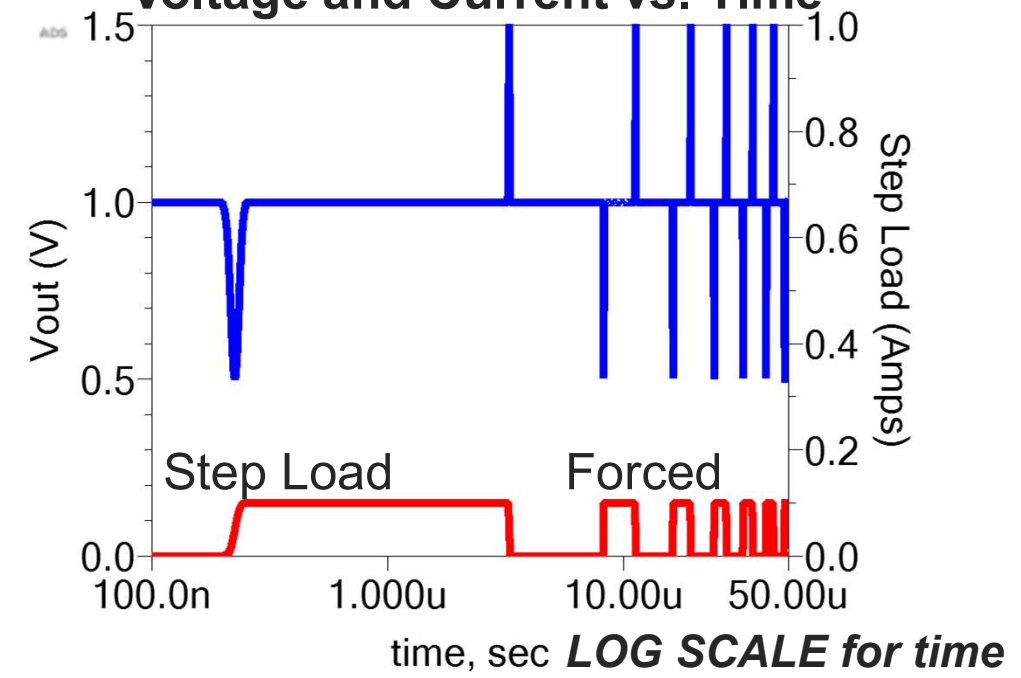
1st Order SOLUTION

Design for Flat Impedance at the output to keep V and I in phase and the feedback stable.

Frequency Domain
Power Supply Output Impedance



Time Domain
Voltage and Current vs. Time



Transition from Power Supply to Bulk Capacitor

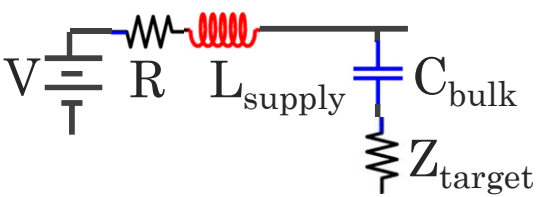
Designing for Flat Impedance

PROBLEM

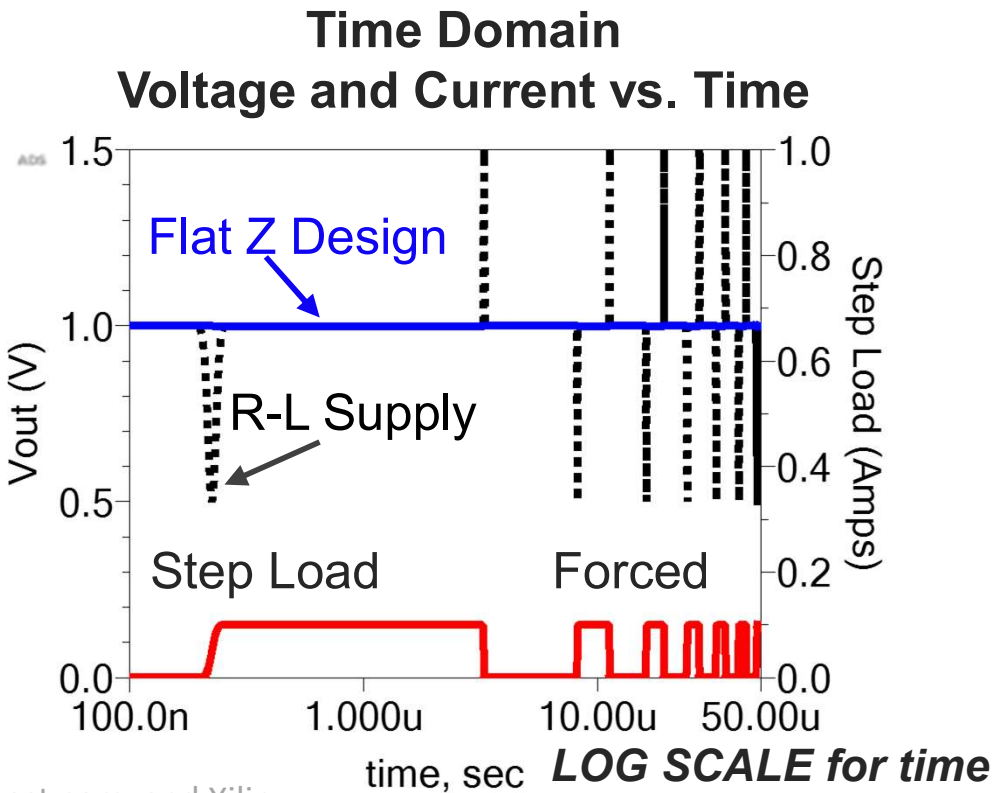
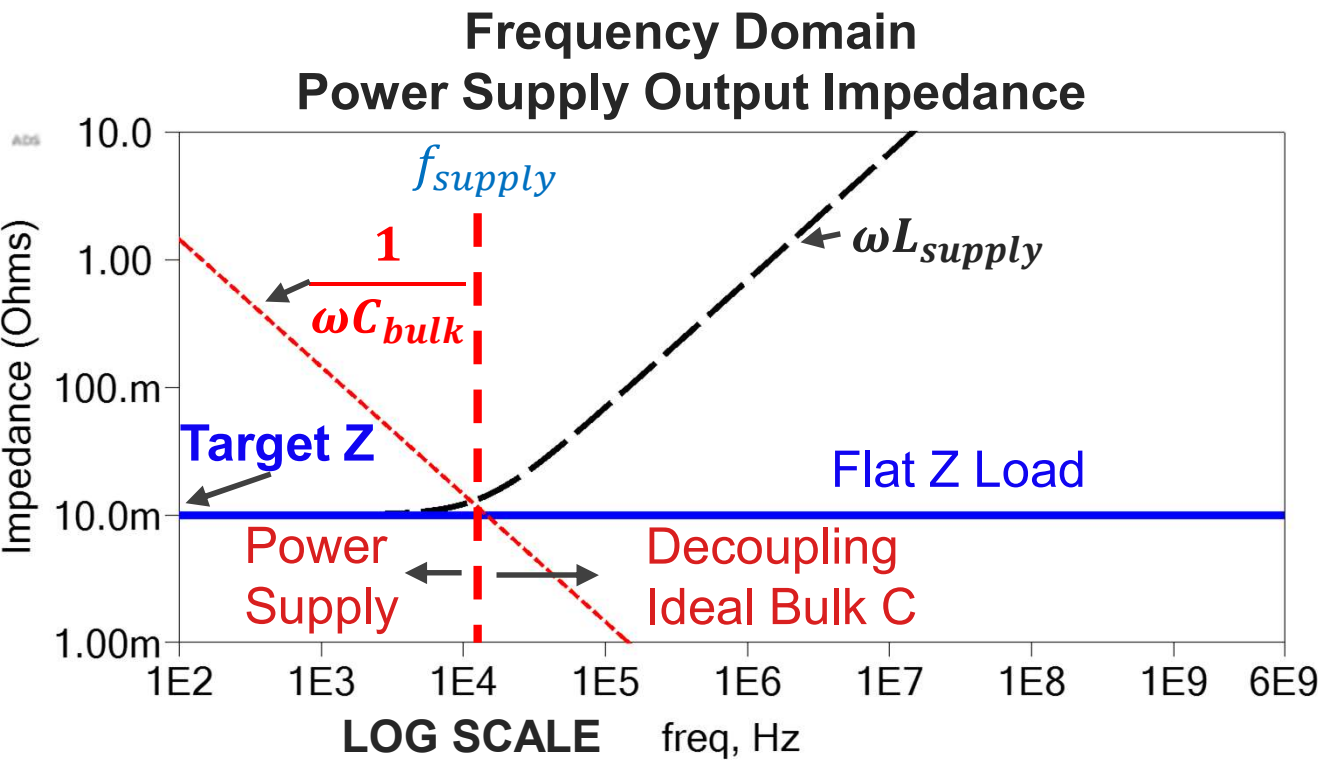
Find the decoupling capacitor that will maintain a Flat Z Load for the Power Supply

1st Order SOLUTION

Add Bulk Capacitor to maintain flat impedance



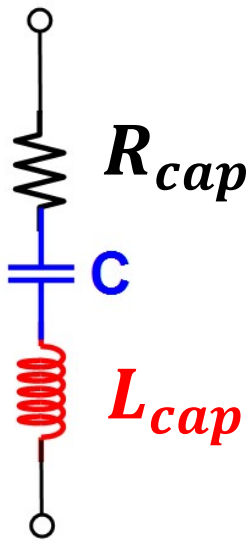
$$C_{bulk} = \frac{L_{supply}}{Z_{Target}^2}$$



Capacitors Have Series L and Series R

Select ESR for Flat Z PDN, Minimize the ESL

Capacitor Model



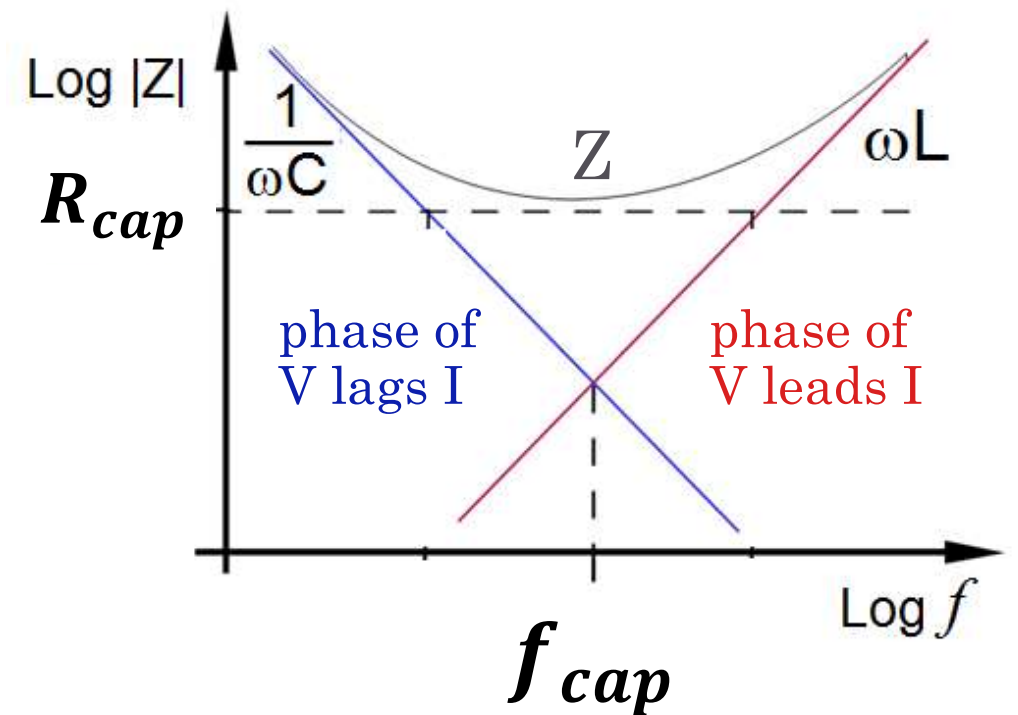
Impedance Equation

$$Z = R_{cap} + \left(j\omega L_{cap} - j\frac{1}{\omega C} \right)$$

$$f_{cap} = \frac{1}{2\pi\sqrt{L_{cap} \times C}}$$

Voltage and current are in phase at f_{cap}

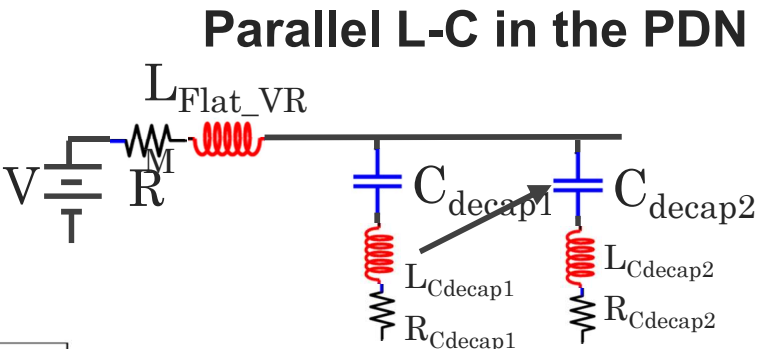
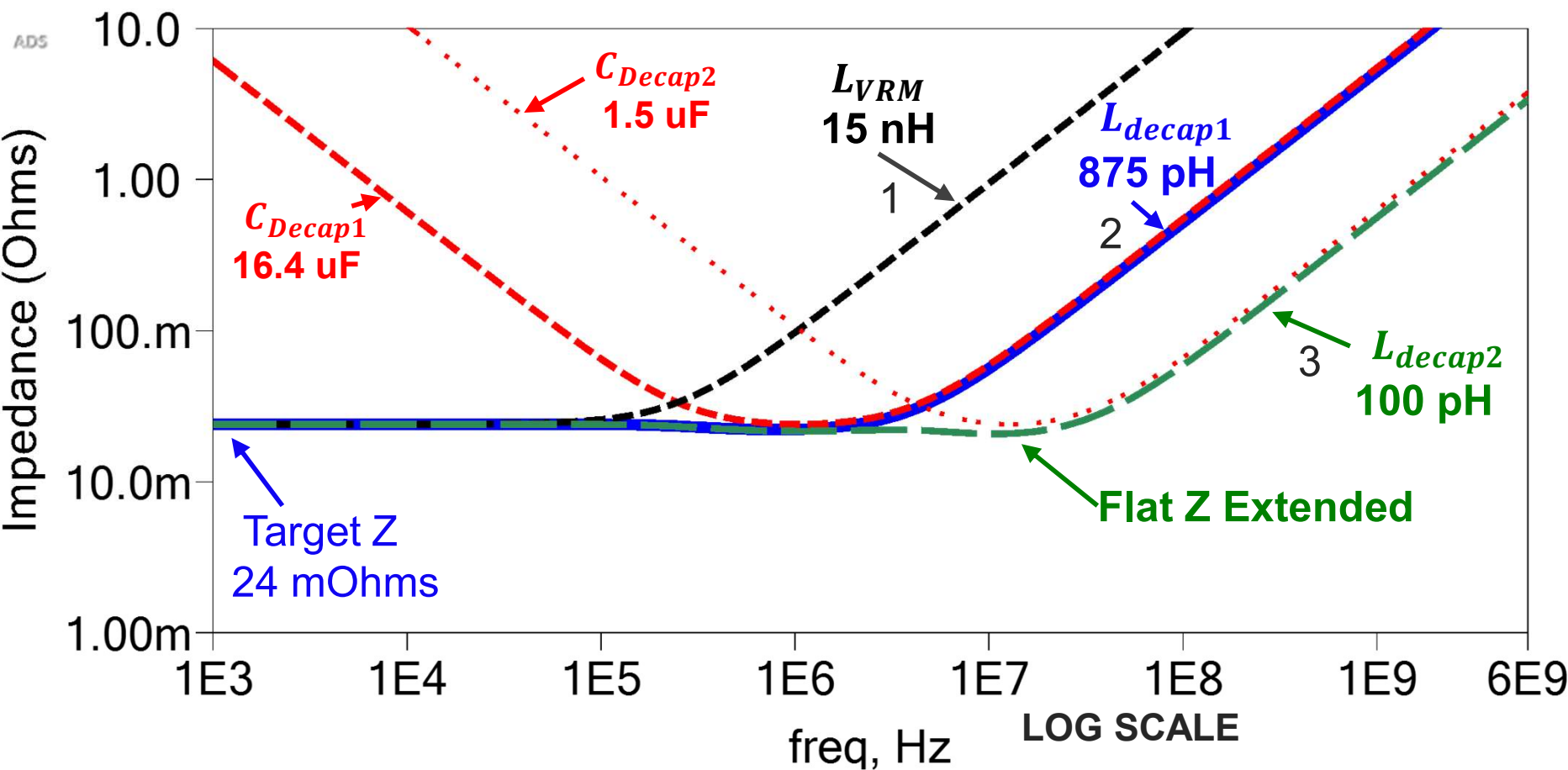
Series RLC Impedance vs. Frequency



Adding Decoupling Capacitors to Reduce L

Smaller Capacitors have Lower ESL

Frequency Domain
Power Supply Output Impedance

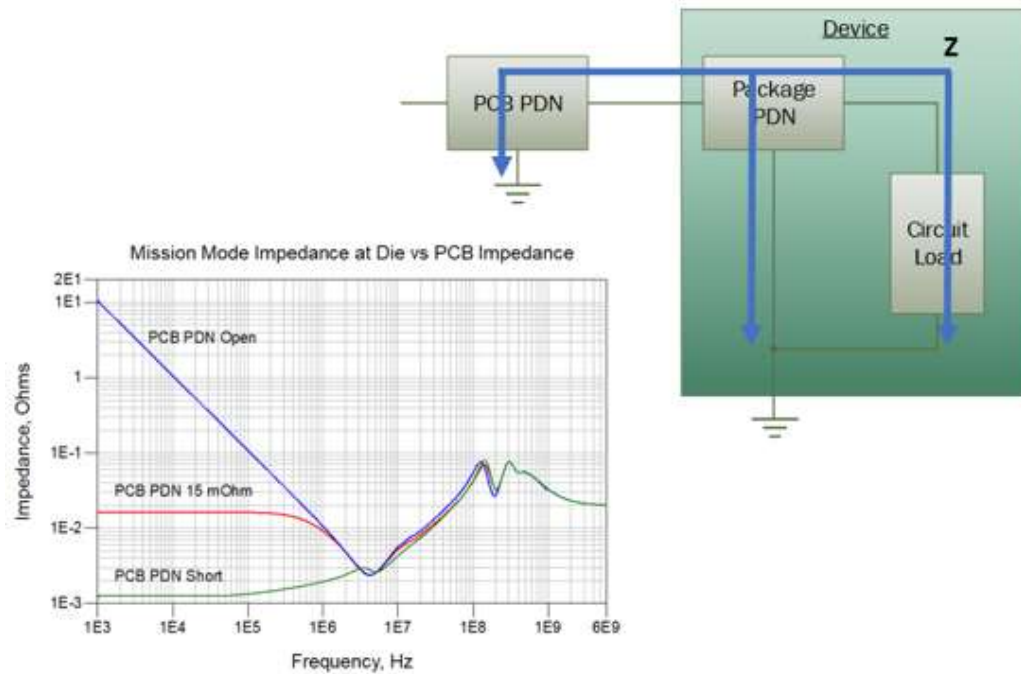


$$C_{decap2} = \frac{L_{decap1}}{Z_{Target}^2}$$
$$= \frac{875pH}{(24\text{ mOhm})^2}$$
$$\approx 1.5\text{ }\mu\text{F}$$

Its about the load and noise sources...

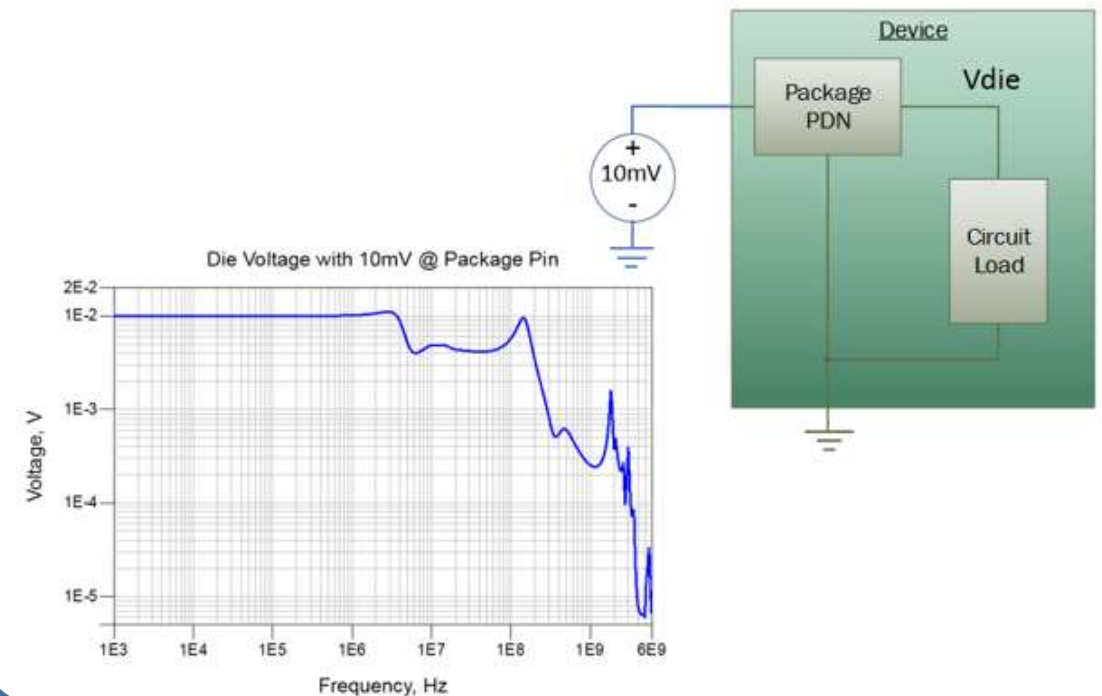
Package/Die S-parameter Model

Power Supply Noise Limits @ Package Ball
Power Supply Noise Spec: 10mV pk-pk



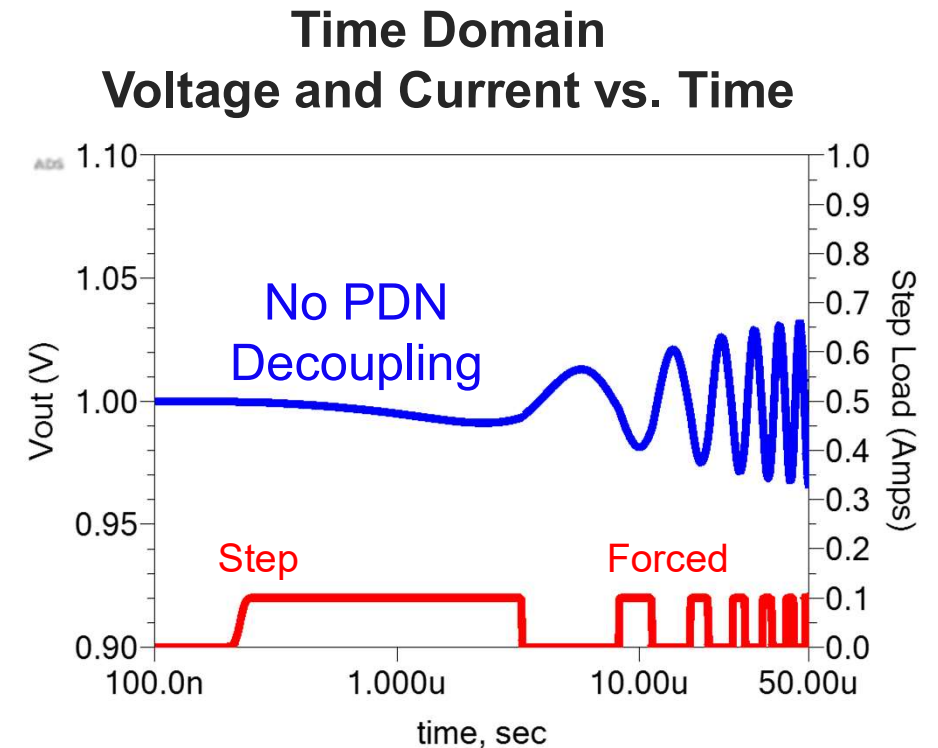
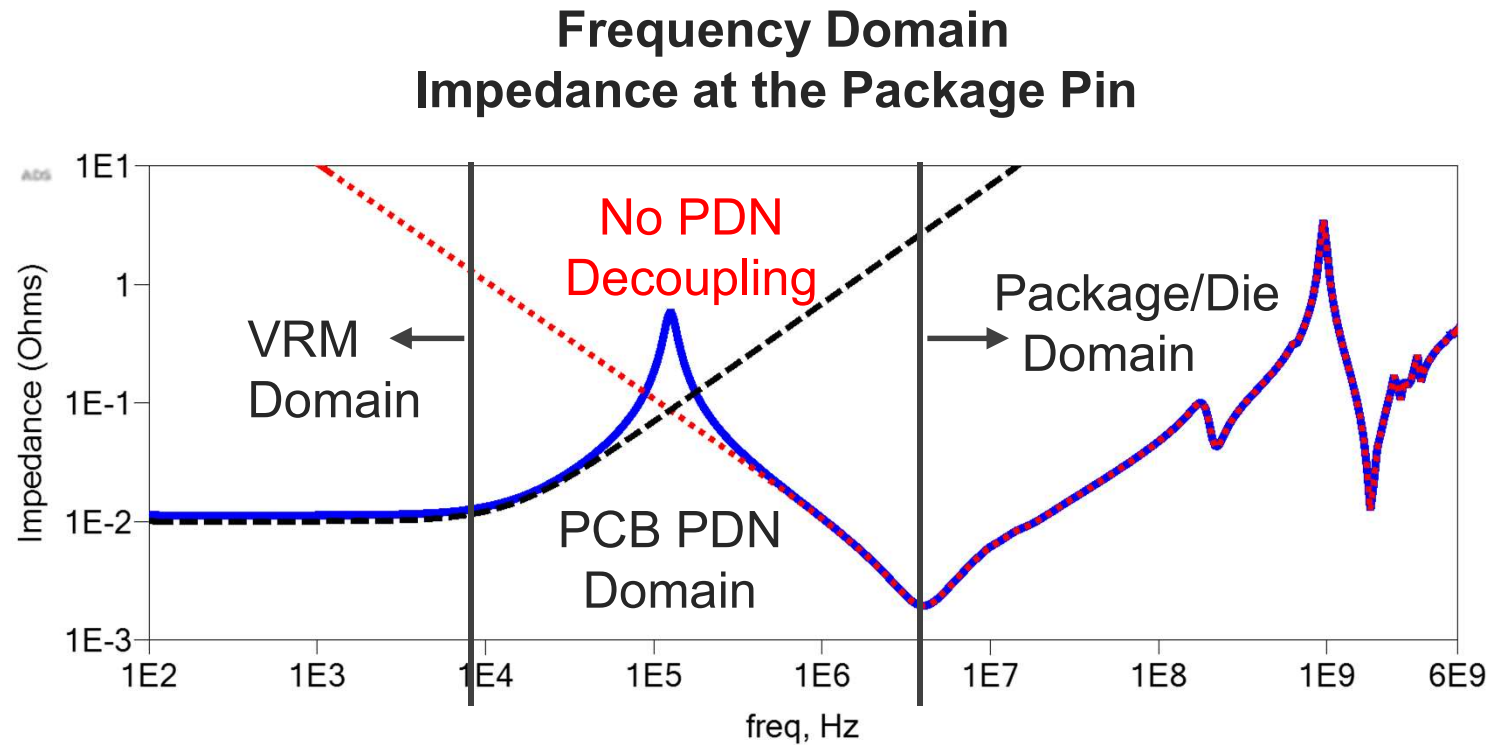
Self-induced [inflicted] noise

External [injected] noise



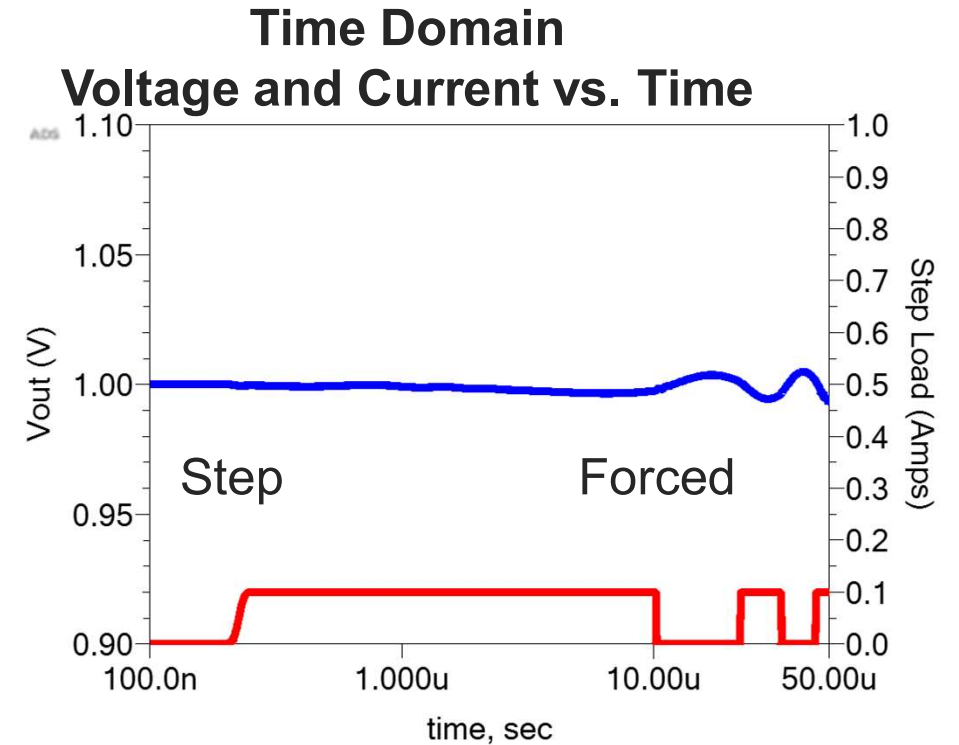
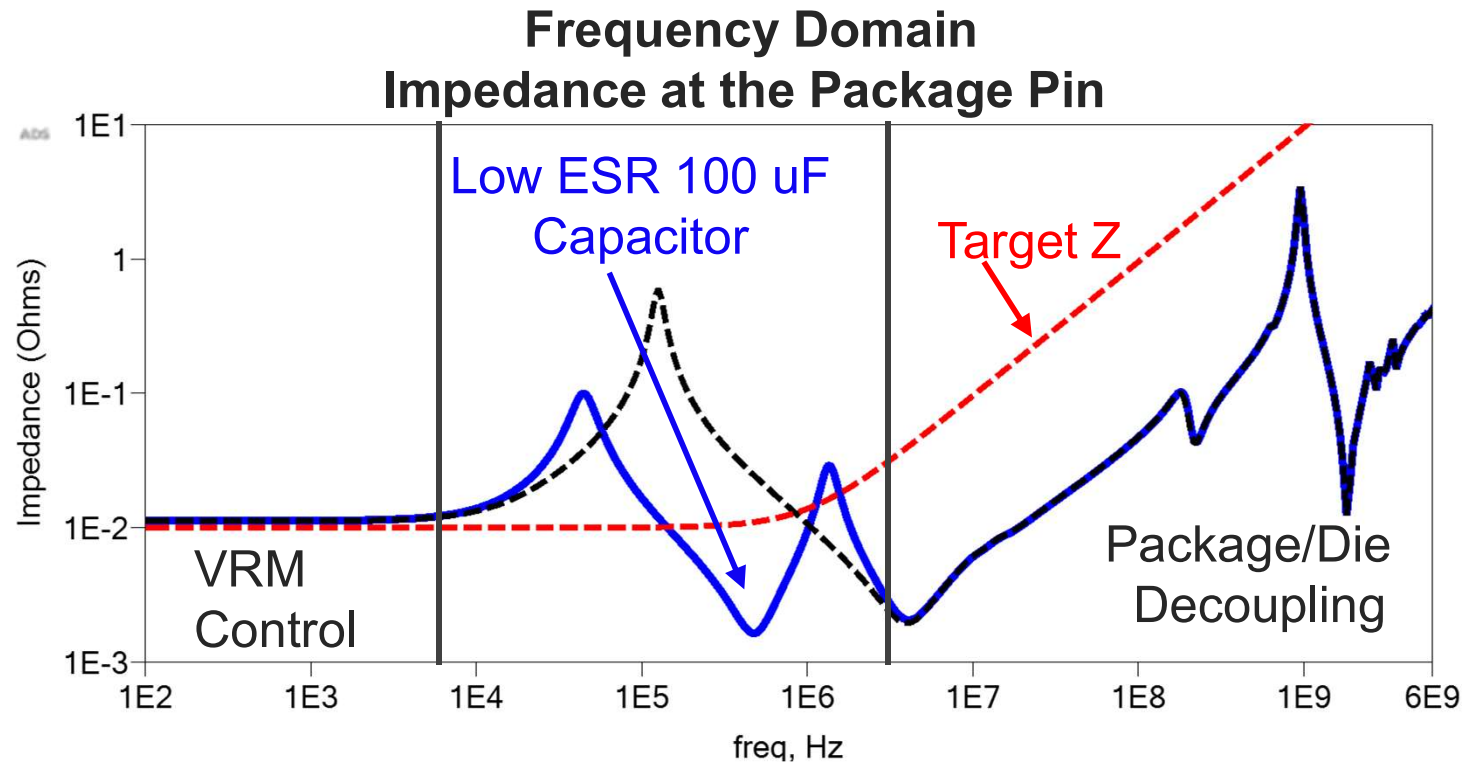
VRM + Load and **No** Decoupling Capacitors

Parallel Resonance Causes Impedance peak



The Wrong Capacitor Can Add Parallel Resonances

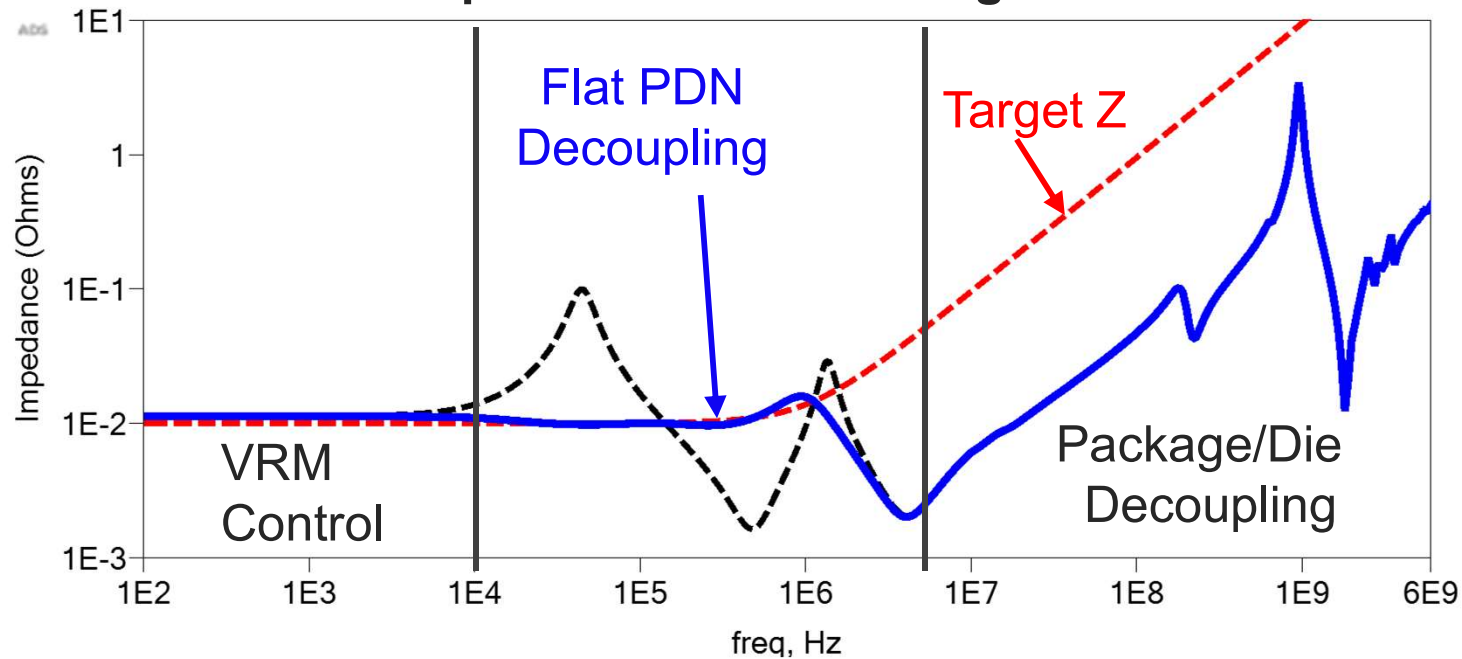
Increases part count to reach target Z



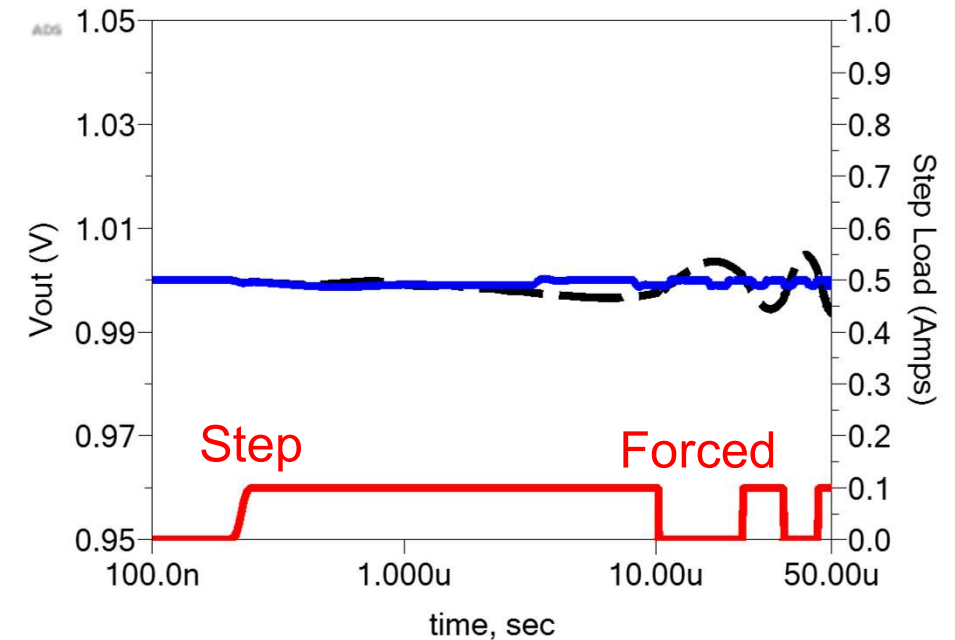
Flat Impedance PDN Design

Flat Z = Maximum Stability, Minimum Ripple, Minimum Capacitors

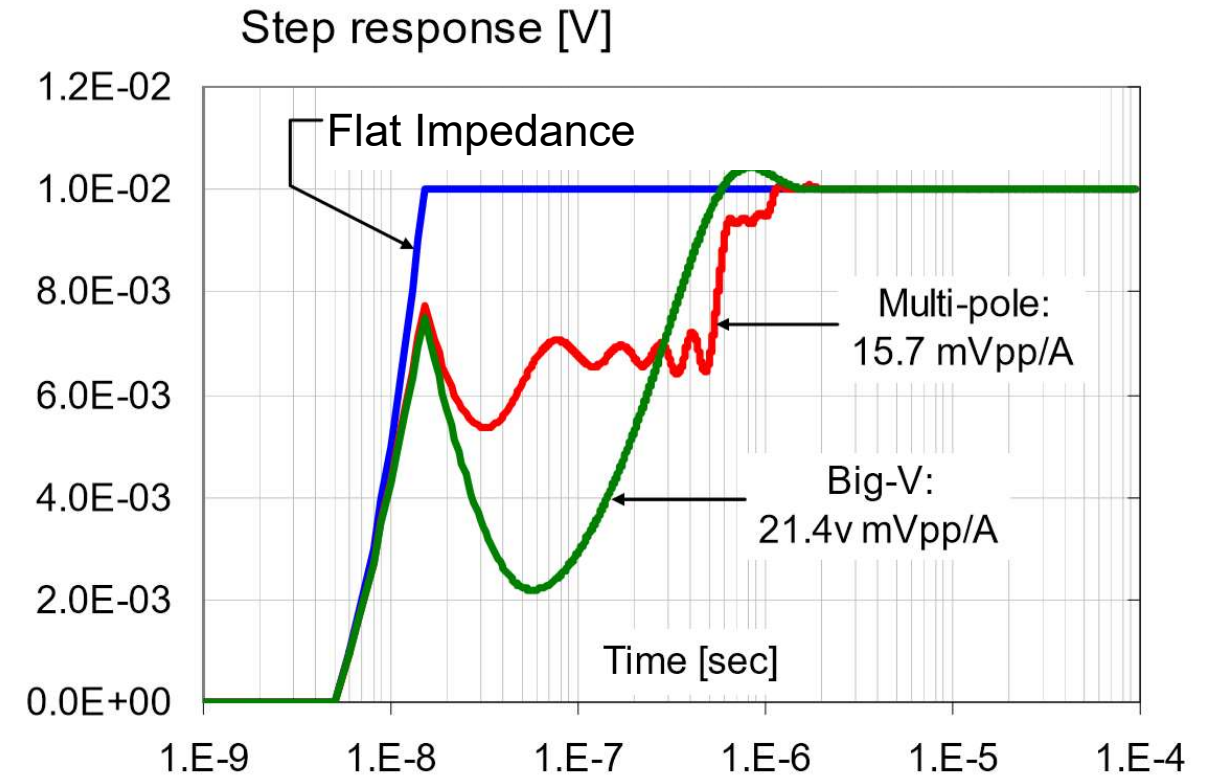
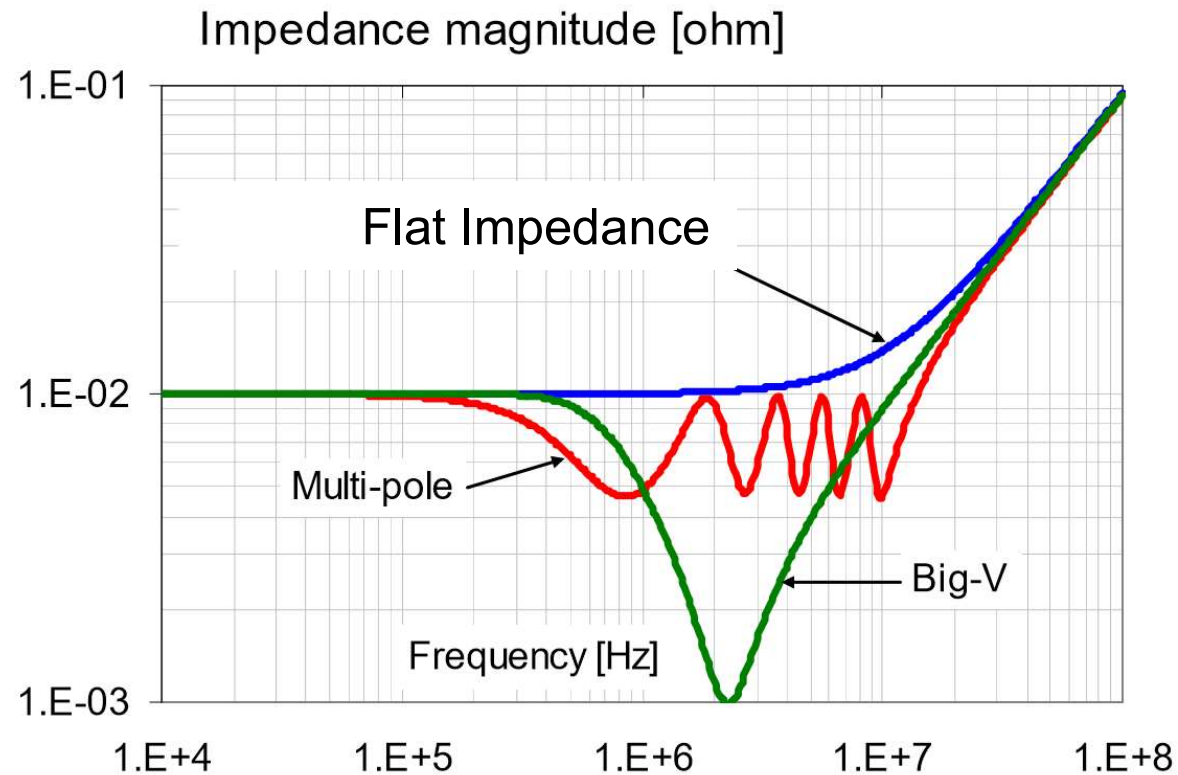
Frequency Domain
Impedance at the Package Pin



Time Domain
Voltage and Current vs. Time



Comparing Decoupling Schemes

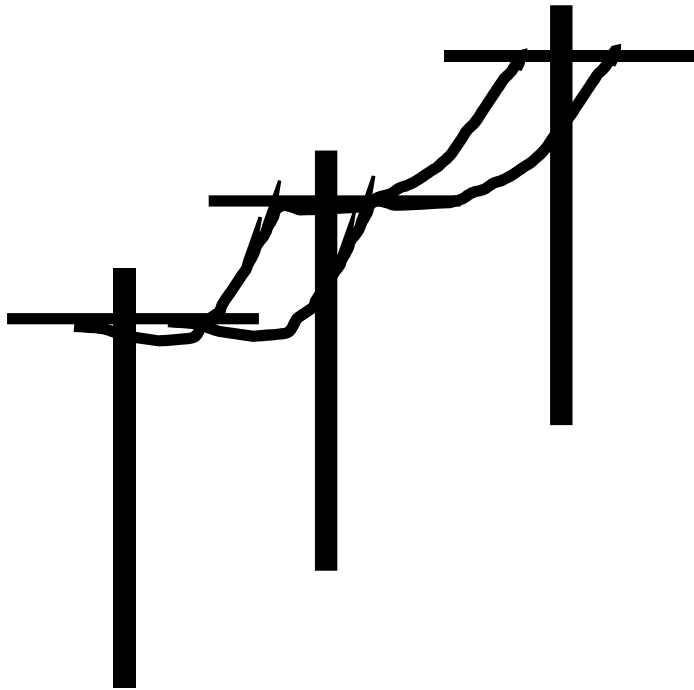


http://electrical-integrity.com/Paper_download_files/DC06_TF-MP3_SUN.pdf

Istvan Novak DesignCon 2006 TF-MP3

History Lesson – The Transatlantic Cable

Engineered design vs. costly debug/redesign



What is so hard about stringing a wire between the transmitter and the receiver?

Where was the SI Engineer in 1858?

Transatlantic telegraph cable

In 1858...signal quality declined rapidly, slowing transmission to an almost unusable speed. The cable was destroyed the following month when Wildman Whitehouse applied excessive voltage to it while trying to achieve faster operation.

Questions For Your Next Design

PI Engineers require simulation and Measurement tools

- Are your designs still leveraging decade capacitor values?
- Are poor designs band-aided with added filters and more capacitors?
- Where is the PI engineer?

3 Step Decoupling Capacitor Optimization

Design Methodology for DeCap Optimization

1. Calculate 1st order approximations using simple resistor, inductor, capacitor **R-L-C** models

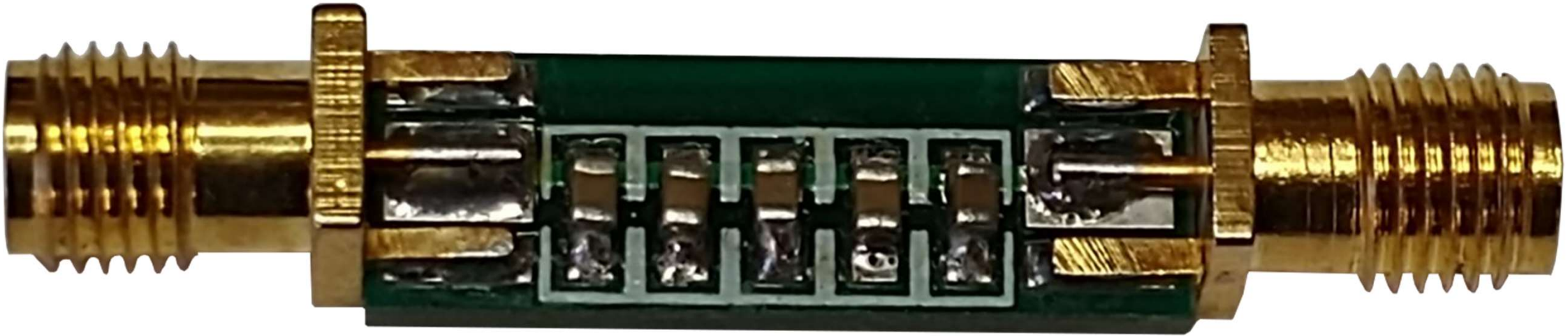


2. Use **Target Z** to optimize the decoupling capacitor selection using high fidelity EM models (**ADS PIPro**)

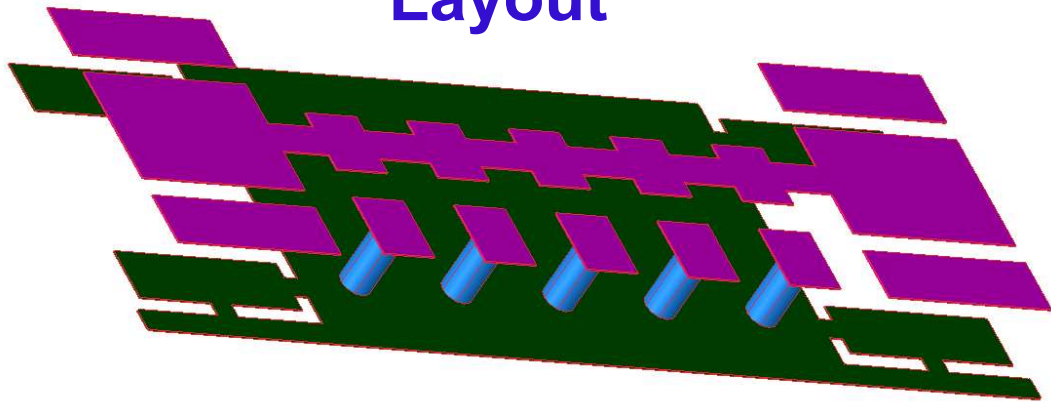
3. Validate with full **Power Integrity Eco-System** simulation in ADS

Why the PI Workflow Needs EM Modeling

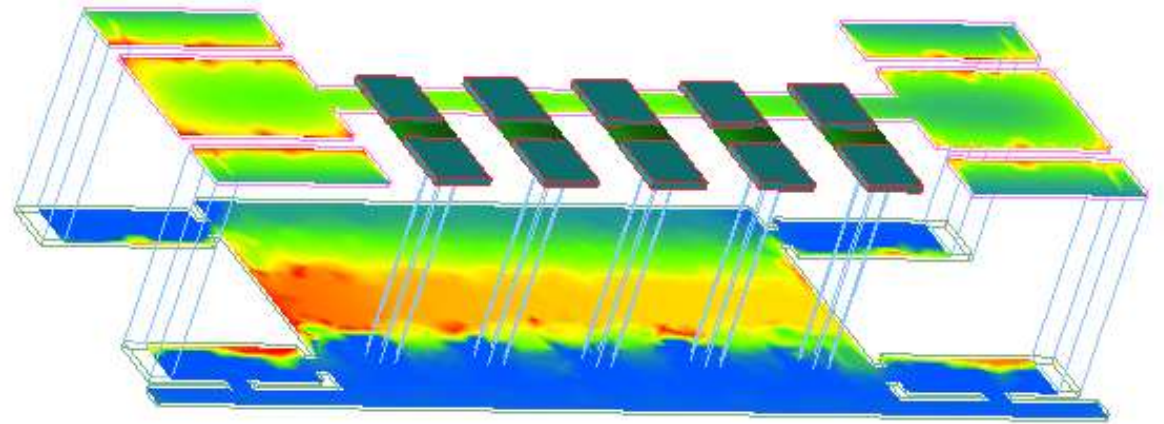
PDN Example of Paralleling 5 capacitors



Layout



EM Simulation with PIPro

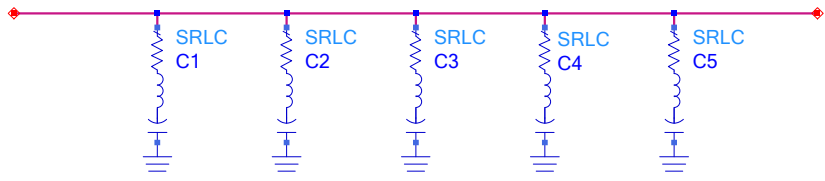


EM Models Capture Real World PCB Parasitics

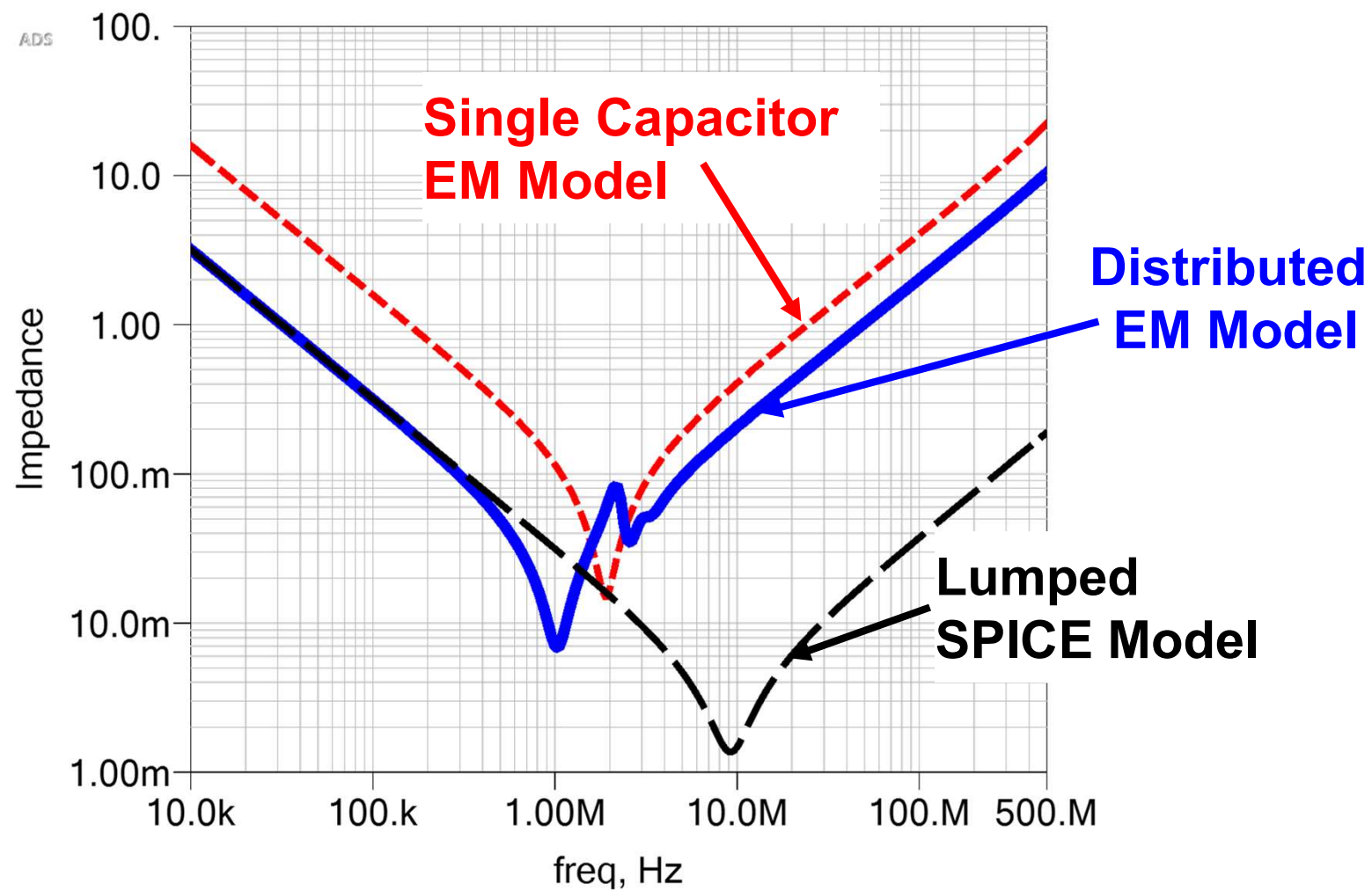
Lumped spice model gets it wrong

Paralleling same value caps

	C	ESR	ESL
C1	1 uF	7 mΩ	300 pH



Parallel Capacitors SPICE vs PCB EM Model

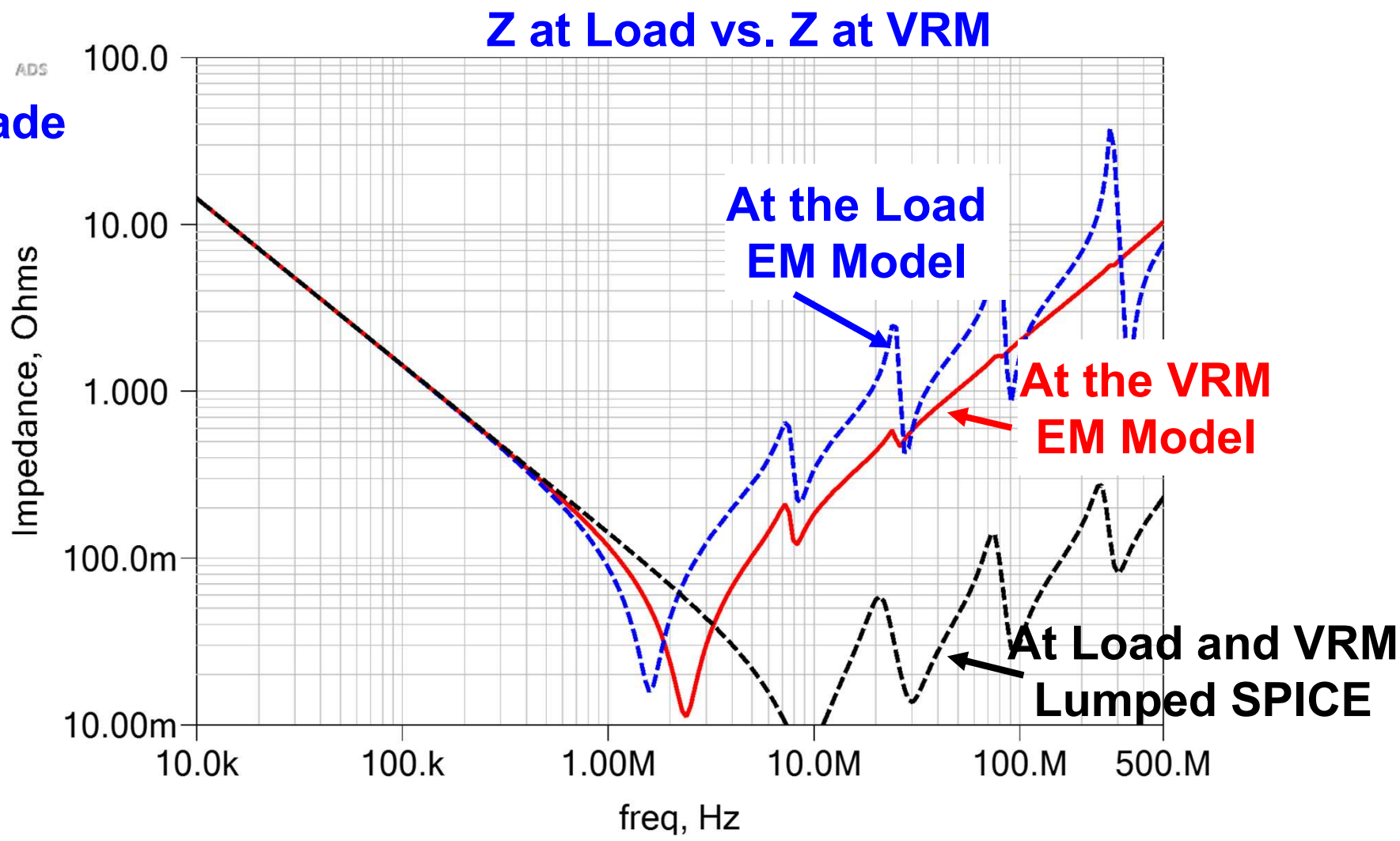
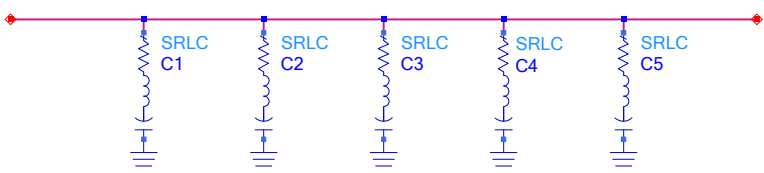


PDN Impedance Depends on the Location

Z at The Load is not the same as Z at the VRM

Capacitor Loading by the Decade

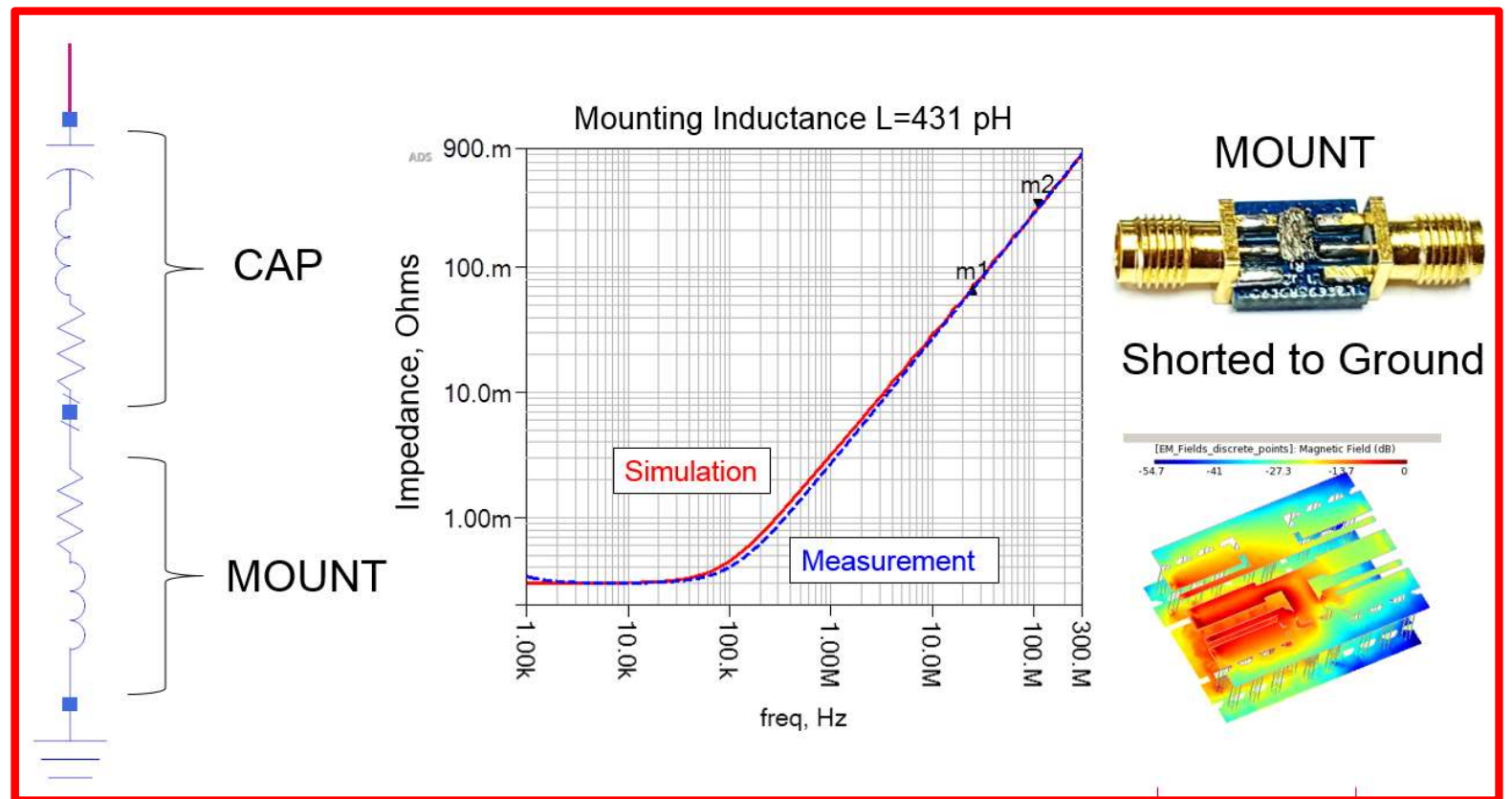
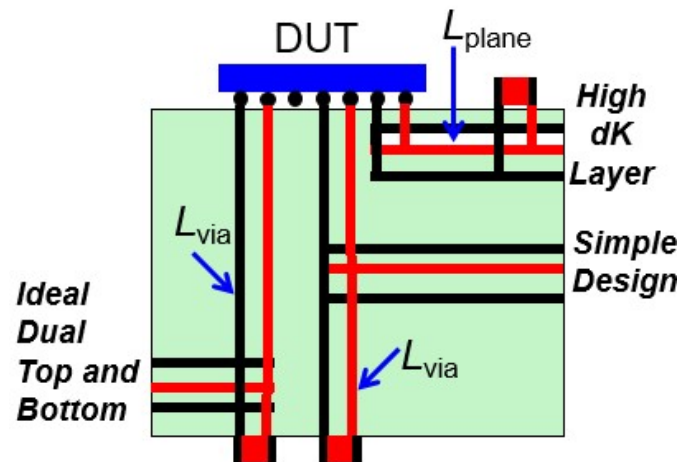
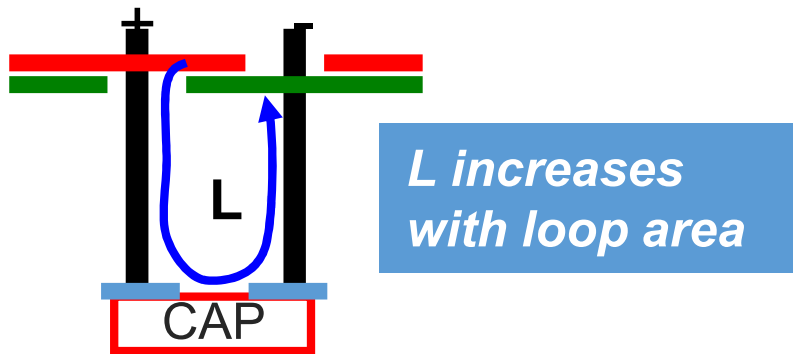
	C	ESR	ESL
C1	1 uF	7 mΩ	300 pH
C2	0.10uF	15 mΩ	300 pH
C3	0.01uF	30 mΩ	300 pH
C4	0.001uF	100 mΩ	300 pH
C5	100pF	200 mΩ	300 pH



PCB Parasitic Inductances are Significant

EM simulators Can Optimize Layout for Low L

Loop Inductance

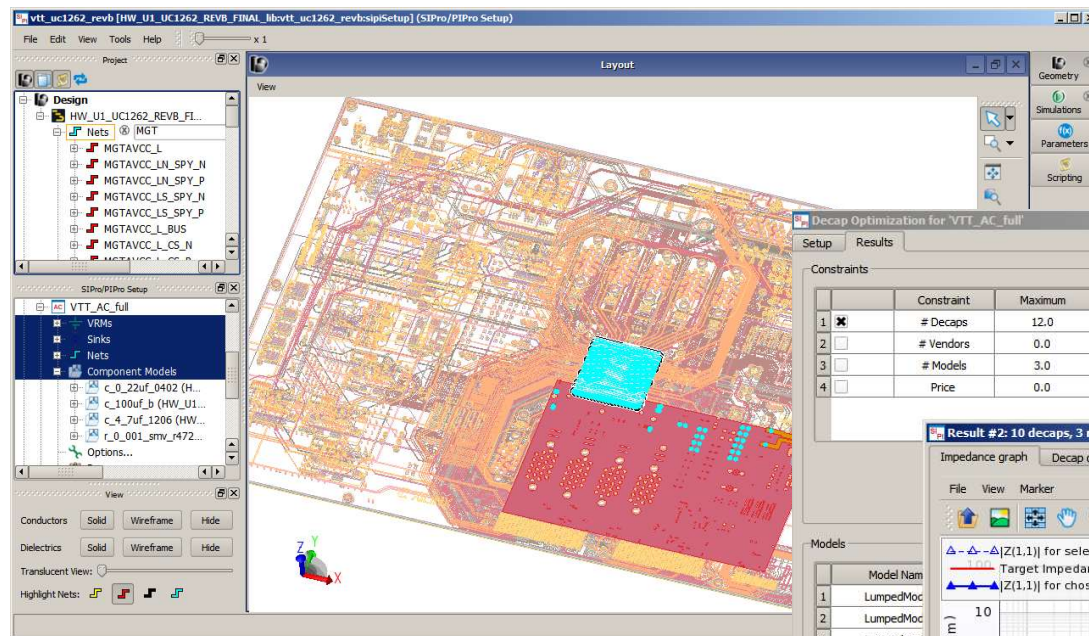


PathWave ADS PIPro EM Simulation of the PCB PDN

Easy setup for high port count simulations

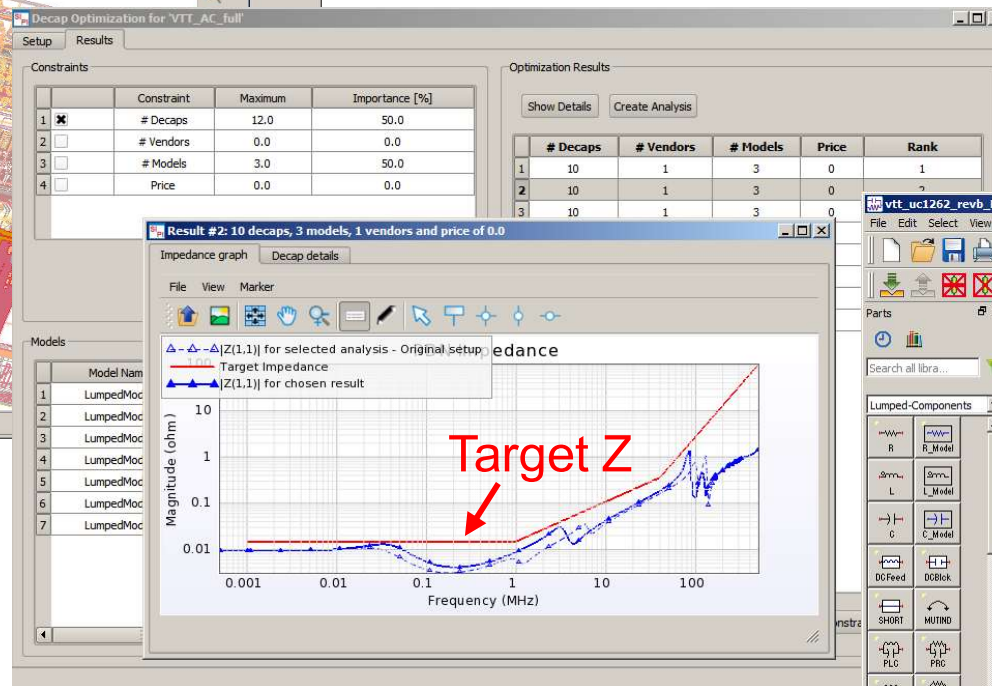
1) IMPORT THE PCB

- Select VRM, Sink, Nets, Components
- Run EM AC Frequency Sweep



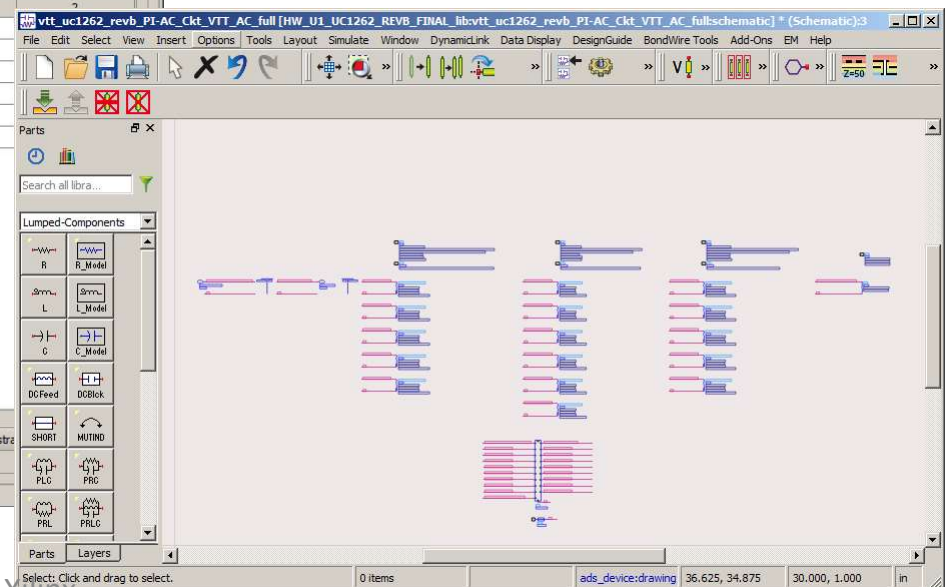
2) OPTIMIZE DECOUPLING

- Select capacitor models
- Setup optimization goals
- Run Optimization



2) GENERATE SCHEMATIC

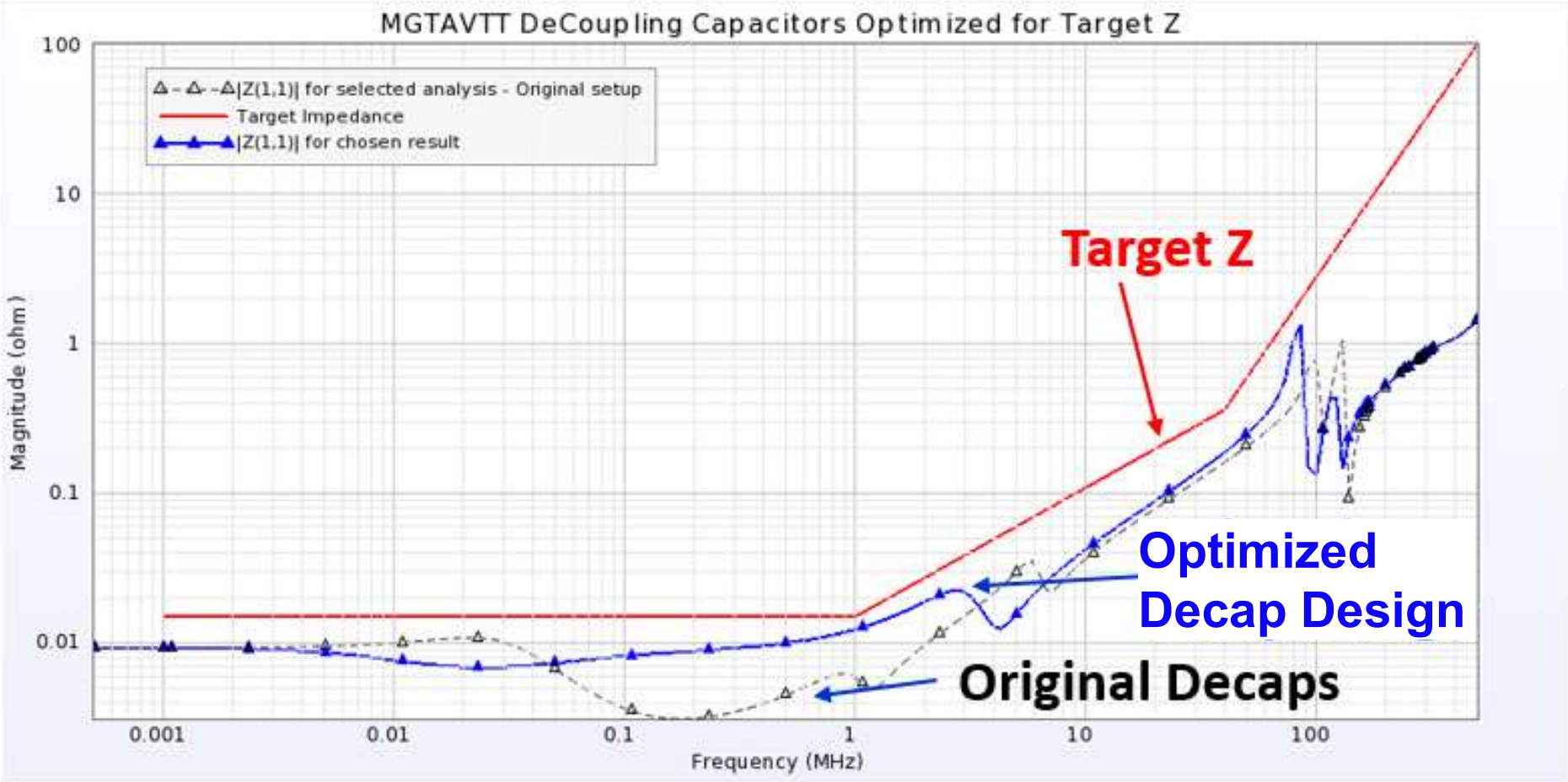
- Auto generate schematic with PCB PDN EM model and optimized capacitors.



Optimize Decoupling for Max Performance/Cost Ratio

Target Z Decoupling Capacitor Optimization

40% Reduction
in Part Count



Capacitors

Yes	C190	330 uF
Yes	C215	330 uF
Yes	C216	330 uF
Yes	C218	330 uF
Yes	C303	220 nF
Yes	C305	220 nF
Yes	C750	220 nF
Yes	C753	220 nF
Yes	C757	220 nF
No	C217	100 uF
No	C225	100 uF
No	C315	4.7 uF
No	C316	4.7 uF
No	C778	4.7 uF
No	C779	4.7 uF
No	C780	4.7 uF

3 Step Decoupling Capacitor Optimization

Design Methodology for DeCap Optimization

1. Calculate 1st order approximations using simple resistor, inductor, capacitor **R-L-C** models
2. Use **Target Z** to optimize the decoupling capacitor selection using high fidelity EM models (**ADS PIPro**)
-  3. Validate with full **Power Integrity Eco-System** simulation in ADS

Voltage Regulator State Spaced Averaged Models

Keysight Youtube video with Steve Sandler of Picotest

Measurement Based VRM Modeling

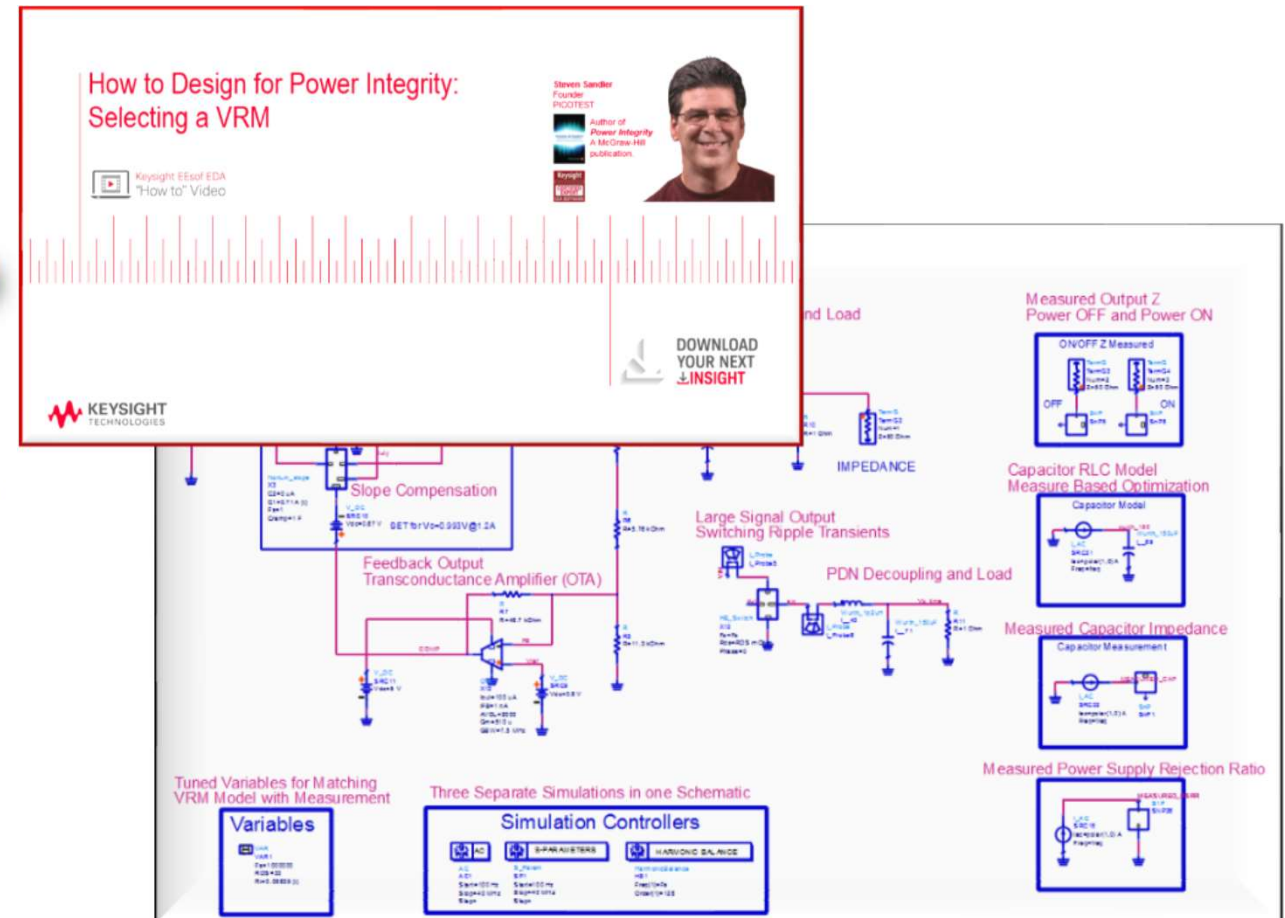


Steve Sandler – PICOTEST



How to Video

<http://tinyurl.com/vrm-video>



Modeling the Power Integrity Ecosystem

VRM + PDN + Load = PI Ecosystem

Three Separate Simulations in one Schematic

Simulation Controllers



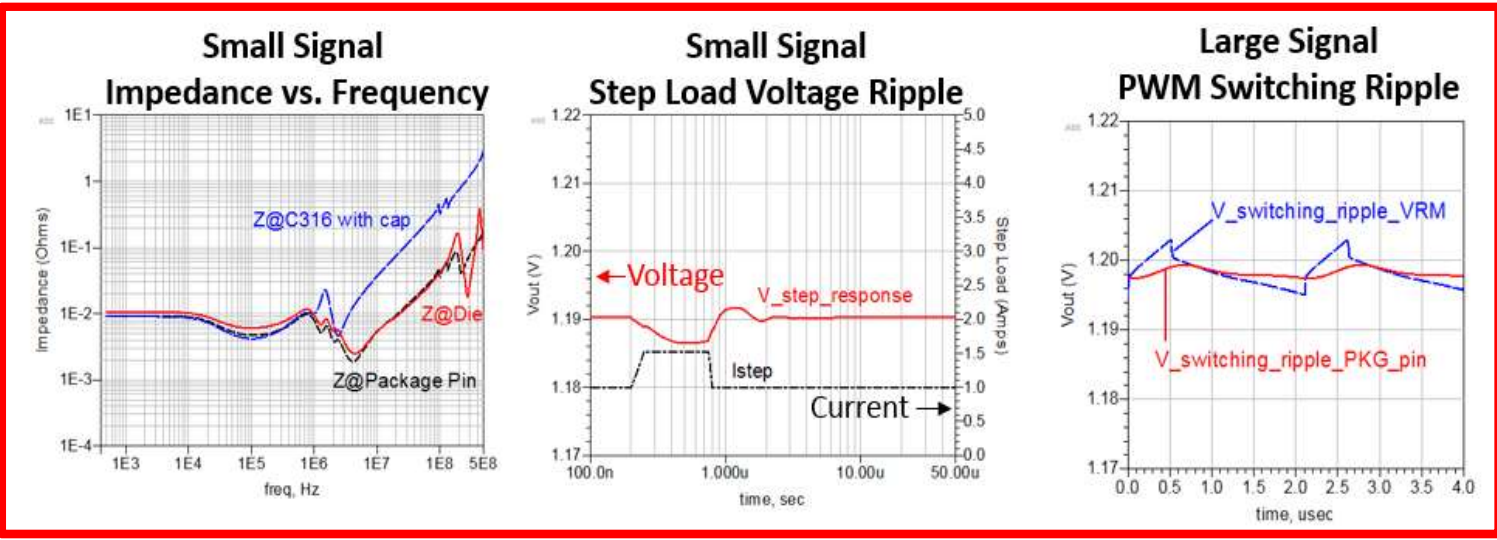
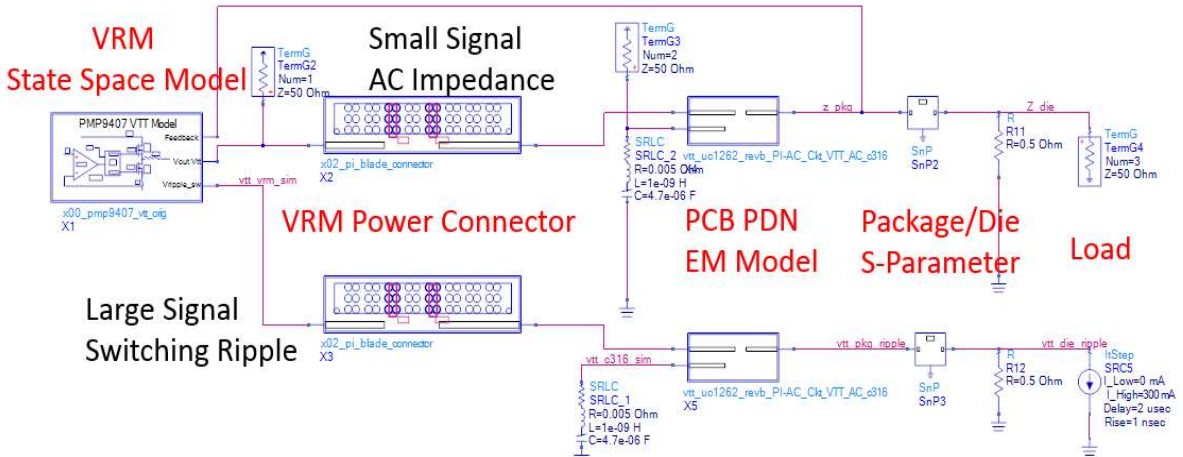
AC
AC1
Start=100 Hz
Stop=40 MHz
Step=



S_Param
SP1
Start=100 Hz
Stop=40 MHz
Step=



HarmonicBalance
HB1
Freq[1]=Fs
Order[1]=256



What We Have Learned

Design Methodology for DecAp optimization

1. Calculate 1st order approximations with **Target Z**

$$C_{bulk} = \frac{L_{supply}}{Z_{Target}^2} \quad C_{decap} = \frac{ESL_{Cbulk}}{Z_{Target}^2} \quad \text{Max } L_{PDN} = C_{pkg} * Z_{Target}^2$$

2. Decoupling capacitor optimization requires **PCB parasitics**
3. **Power Integrity Eco-System** includes switching **VRM models**

How to Design for Power Integrity 5 Part Series on YouTube

with PI expert Steve Sandler

1

How to Design for Power Integrity:
Finding Power Delivery Noise Problems



Steven Sandler
Founder
PICOTEST
Author of
Power Integrity
A McGraw-Hill
publication.



Keysight EEsof EDA
"How to" Video



2

How to Design for Power Integrity:
Selecting a VRM



Steven Sandler
Founder
PICOTEST
Author of
Power Integrity
A McGraw-Hill
publication.



Keysight EEsof EDA
"How to" Video



3

How to Design for Power Integrity:
Measuring, Modeling, Simulating
Capacitors and Inductors



Steven Sandler
Founder
PICOTEST
Author of
Power Integrity
A McGraw-Hill
publication.



Keysight EEsof EDA
"How to" Video



4

How to Design for Power Integrity:
DC-DC Converter Modeling and Simulation



Steven Sandler
Founder
PICOTEST
Author of
Power Integrity
A McGraw-Hill
publication.



Keysight EEsof EDA
"How to" Video



5

How to Design for Power Integrity:
Optimizing Decoupling Capacitors



Steven Sandler
Founder
PICOTEST
Author of
Power Integrity
A McGraw-Hill
publication.



Keysight EEsof EDA
"How to" Video





Hands-On Lab 1:

200128_PI_Lab1_Impedance_wrk.7zads

Basics – Instructor Led Demo

Target Z: LC Parallel Resonance and Calculating C for Flat Z

Explore –

Parallel Capacitors: Lumped SPICE vs. Distributed PCB EM Model

Advanced –

Worst Case Rogue Waves: Frequency Domain Impedance in the Time

Thank You!

■ ■

Questions?